RF Circuit Design in Nanometer CMOS

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Outline

- Introduction
  - RF System trend
  - CMOS Technology trend
- Circuit Innovations
  - Noise canceling
  - 1/f noise reduction
  - Distortion canceling
  - Switched Gm mixer

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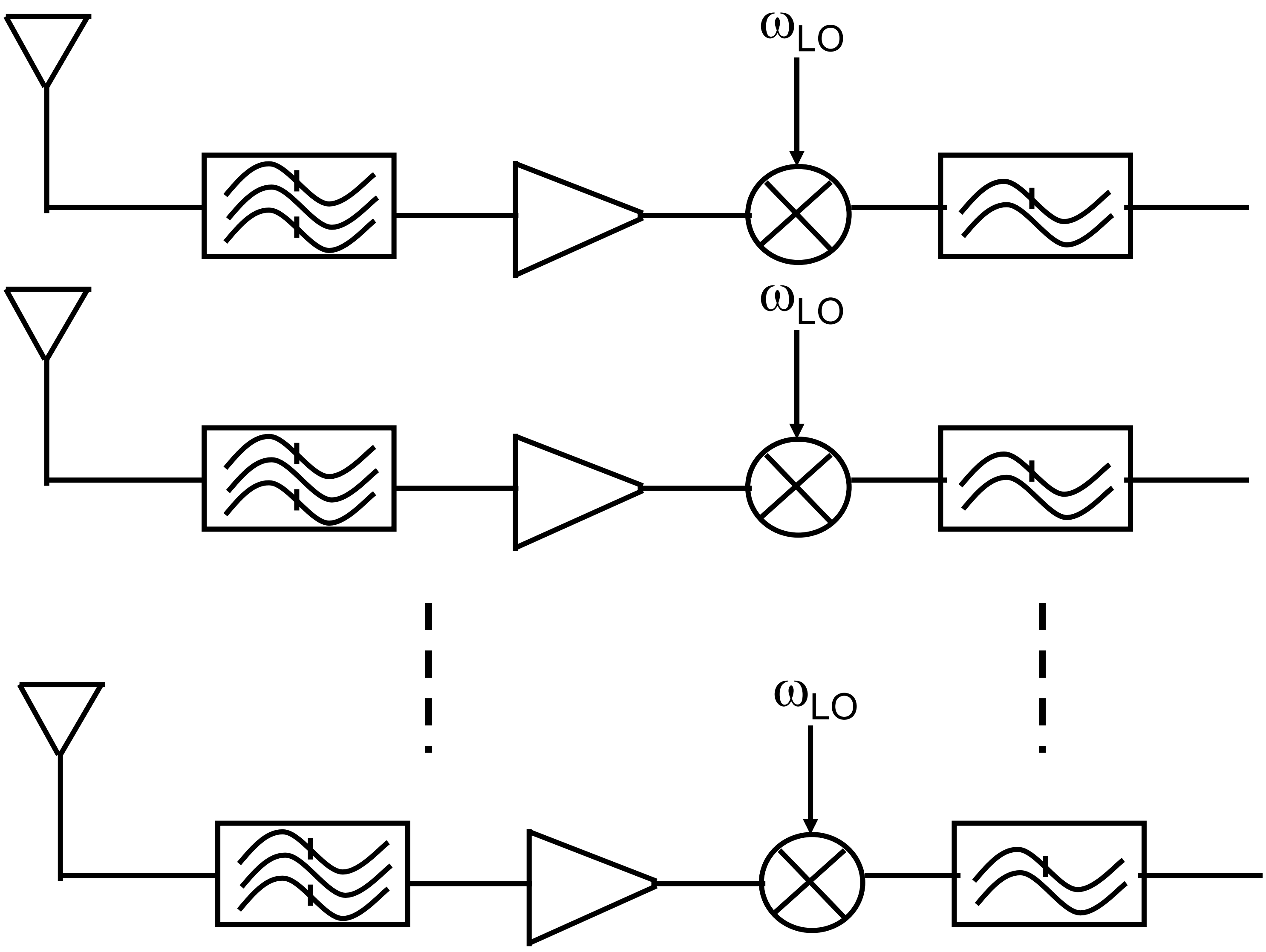
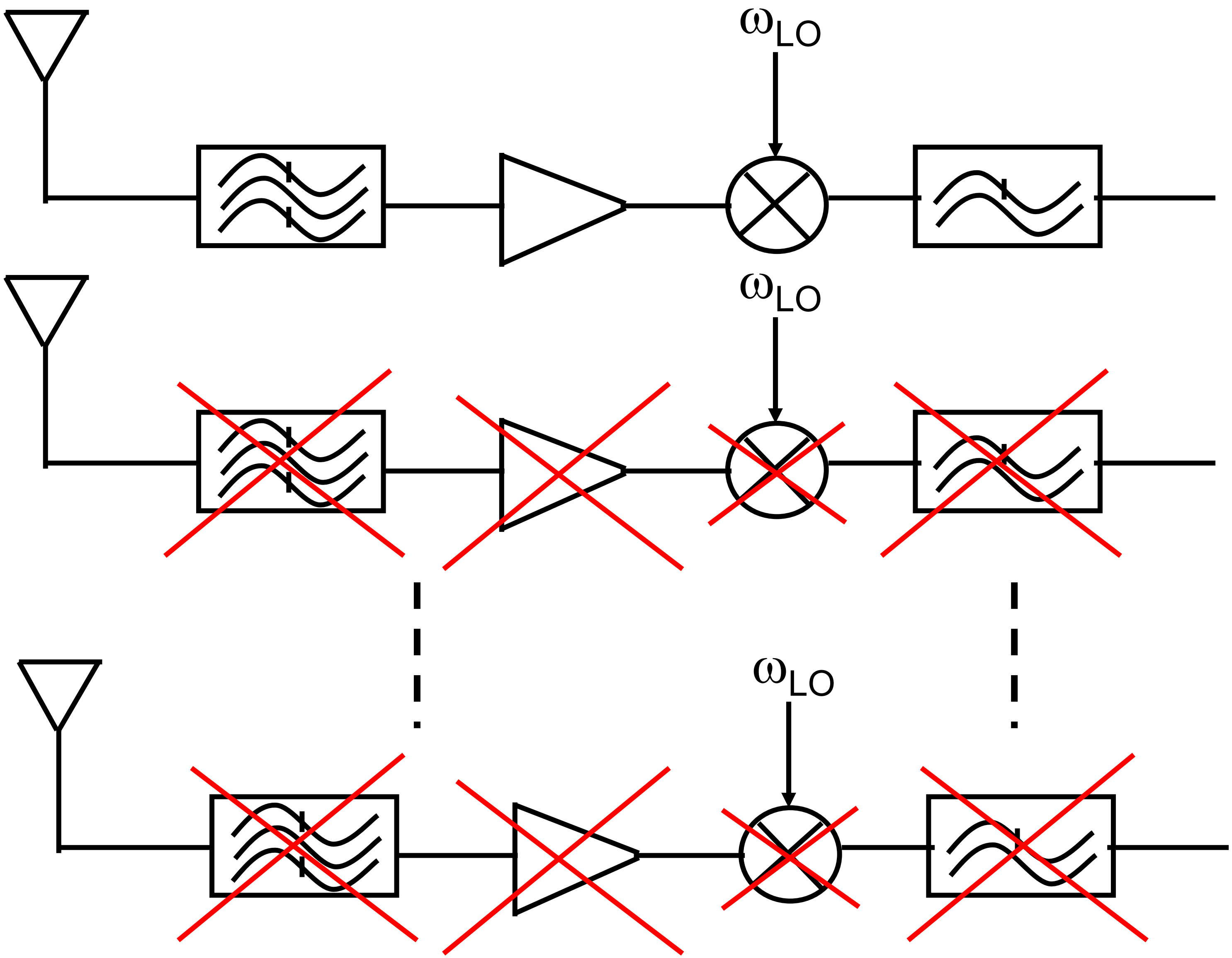
RF system trend

- Many radio standards in one device
- Low cost & small form factor
- All CMOS!

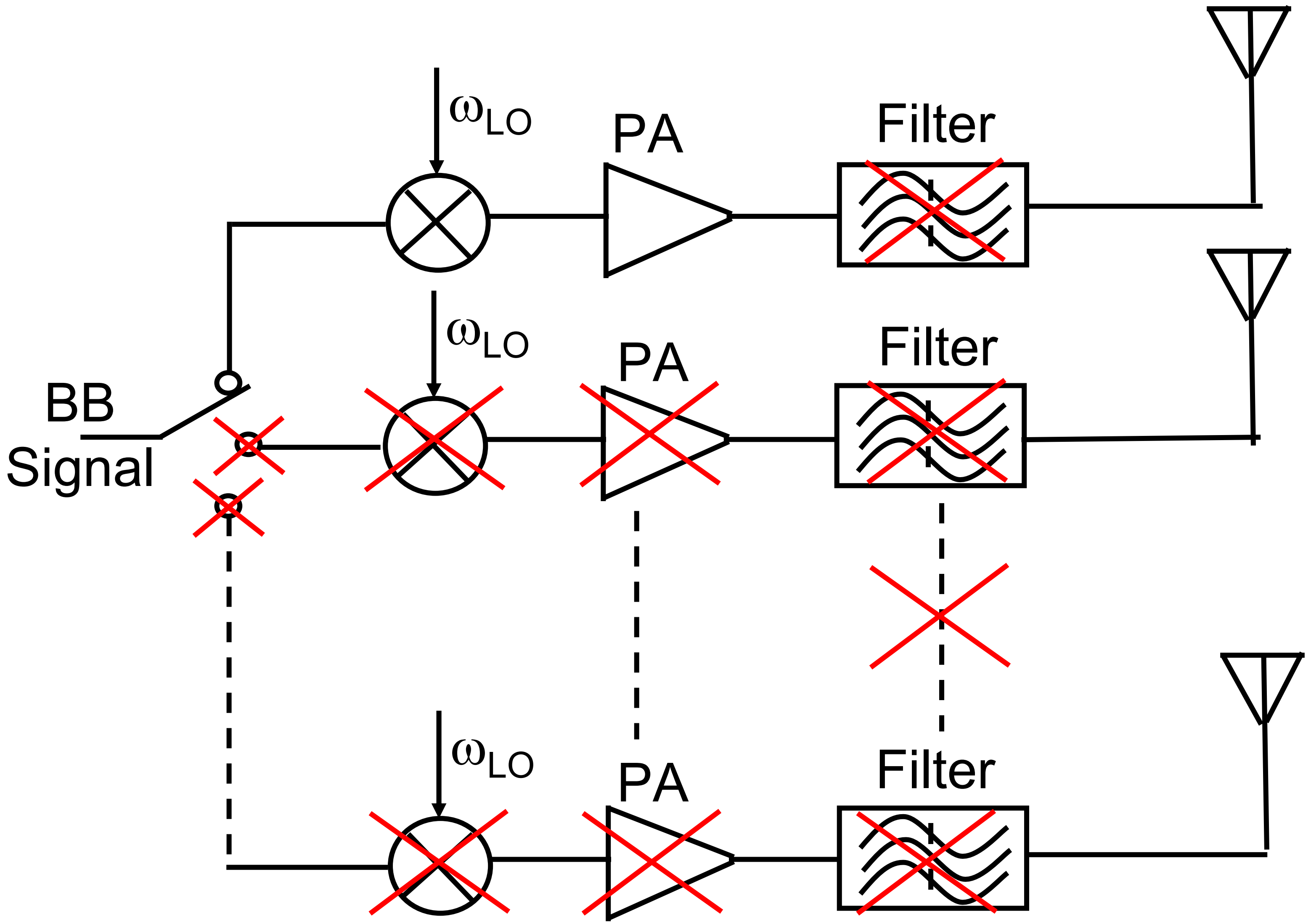
Many Frontends in one device:



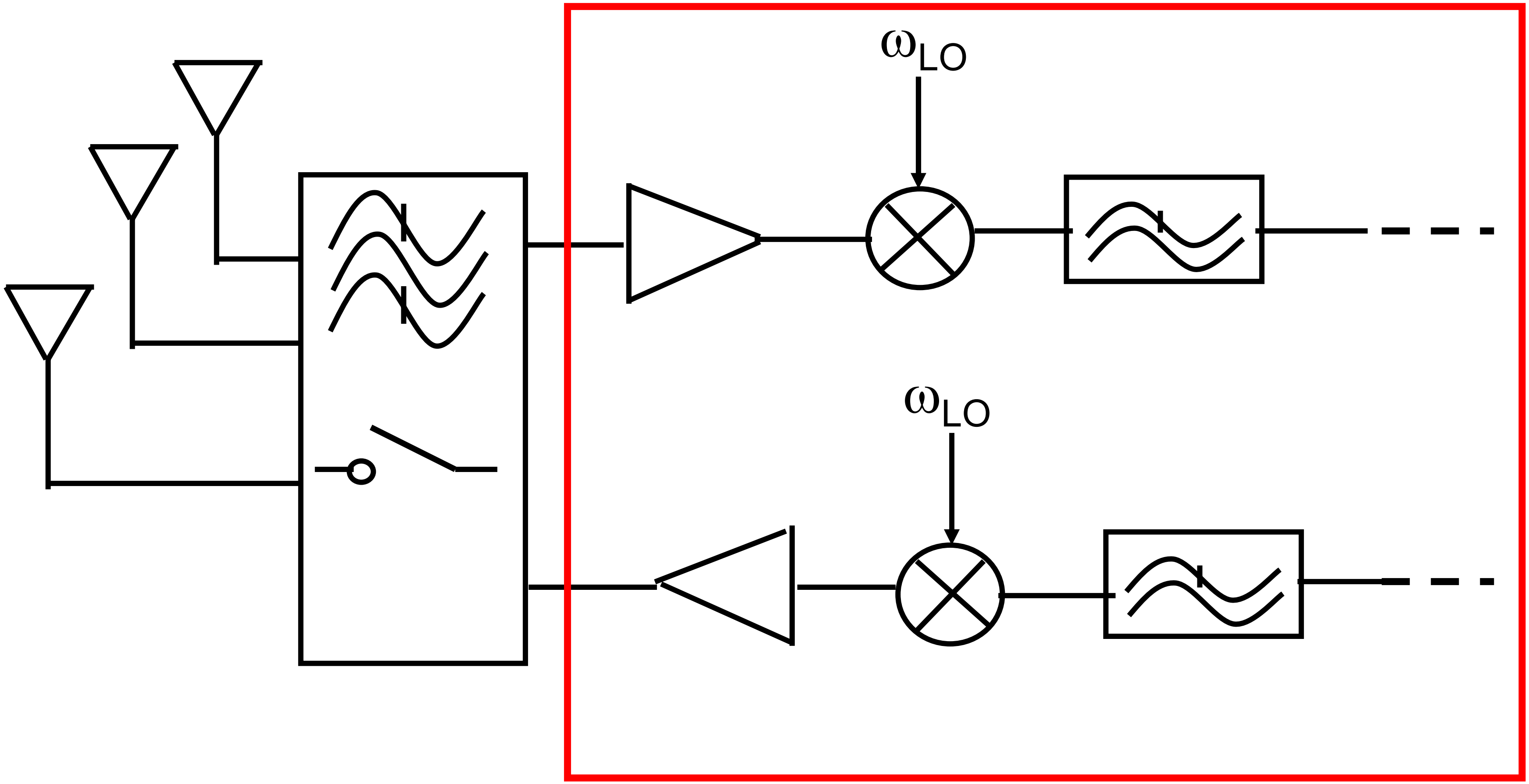
Many Frontends in one device:



Same problem at TX



Preferred: one wide band frontend IC:



RF system trend

- Challenges wide band circuits:

Minimal pre-filtering: → high linearity
No high Q tanks: → low noise

- Bandwidth will be ok for low GHz

- Towards Software Defined Radio

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CMOS Technology trend

- Today 90/65 nm in mass production
- Down to 45 nm planar bulk device
- Below 45 nm: maybe alternative (FinFet)
- What about the analog/RF properties?

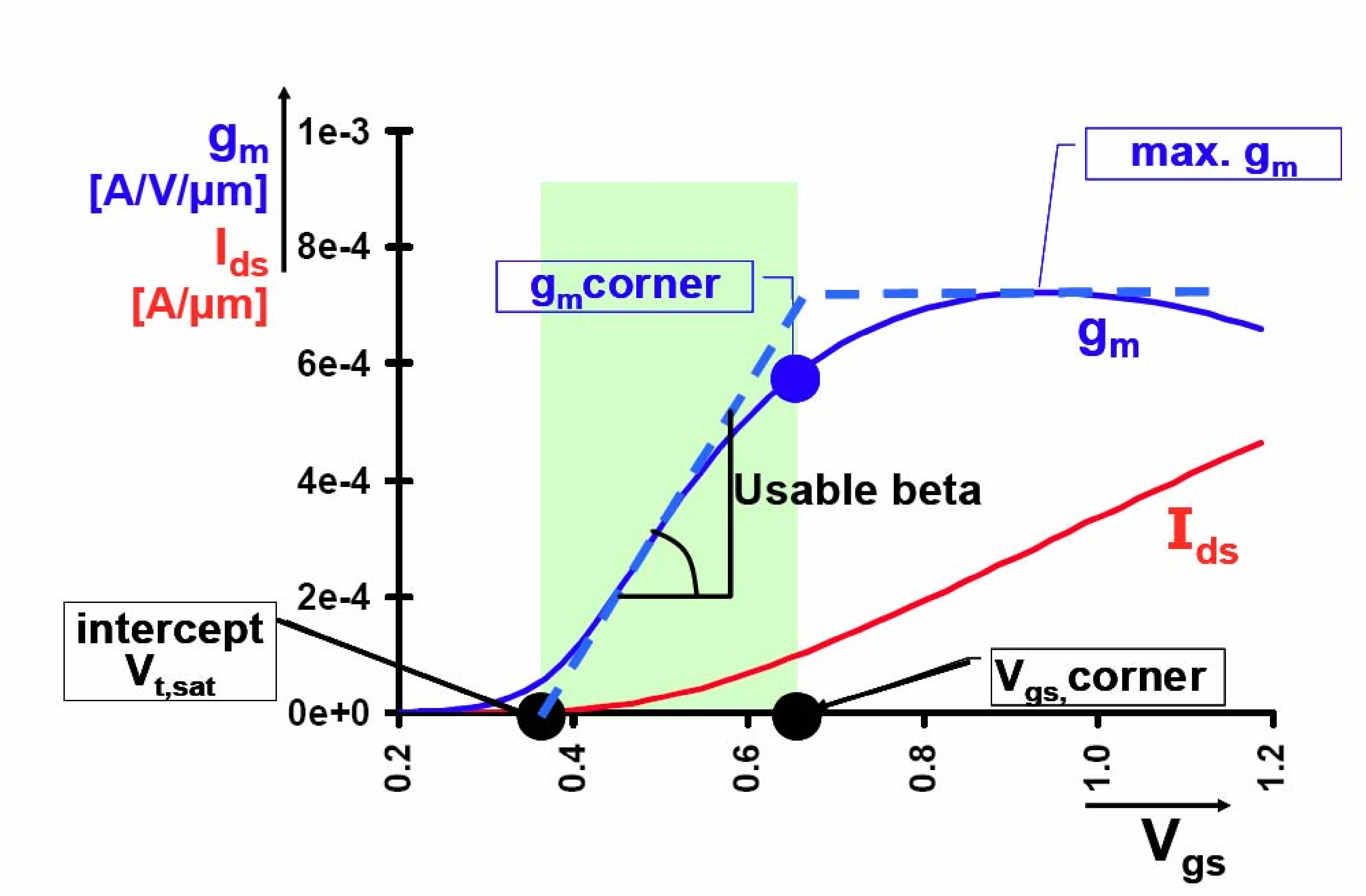
Technology scaling, good news

- **AC**: faster

Technology scaling, bad news

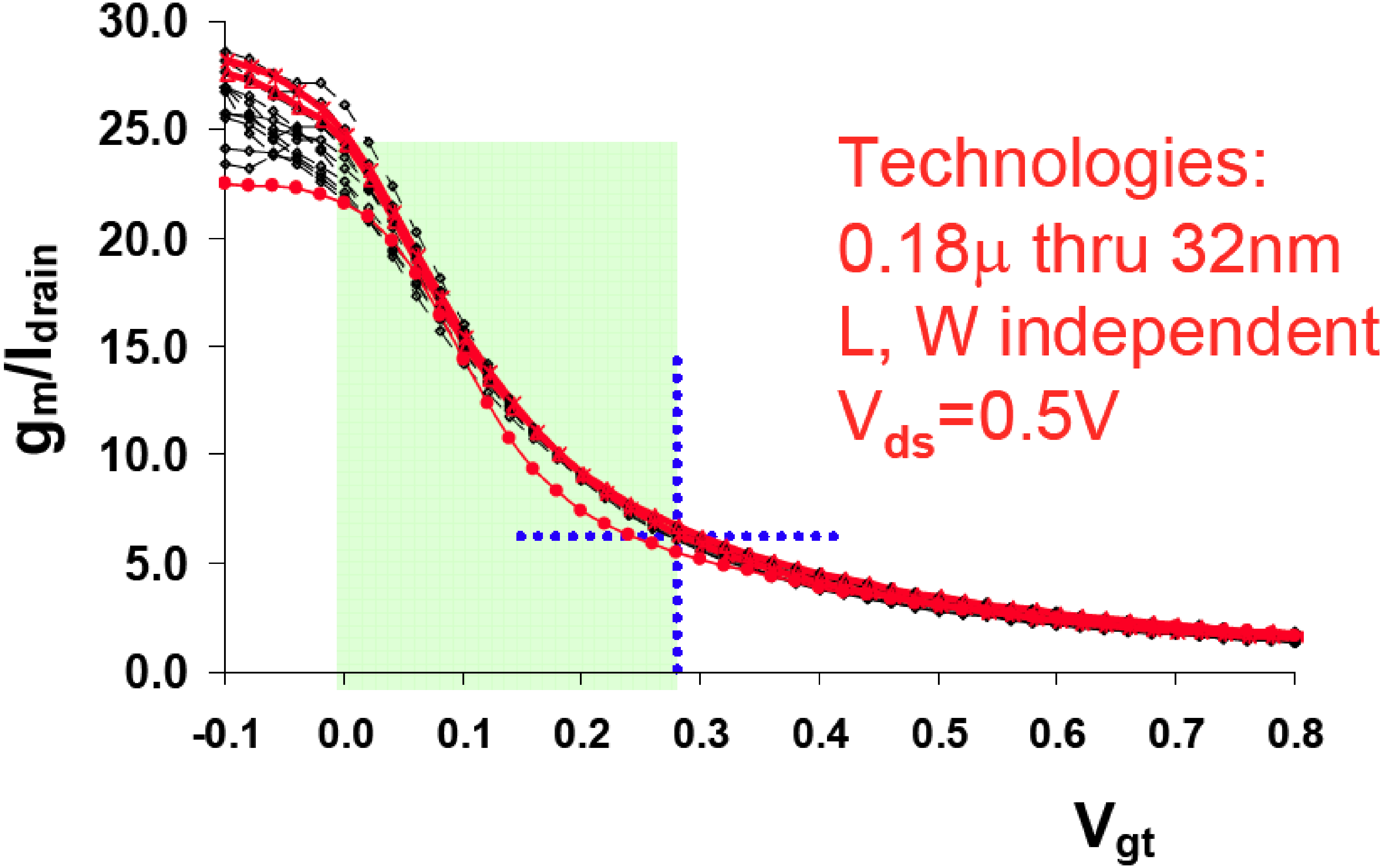
- Id (Vgs) Characteristic -> gm
- Id (Vds) Characteristic -> output conductance
- Gate leakage
- Low voltage operation

V_{gs}-I_d characteristic:



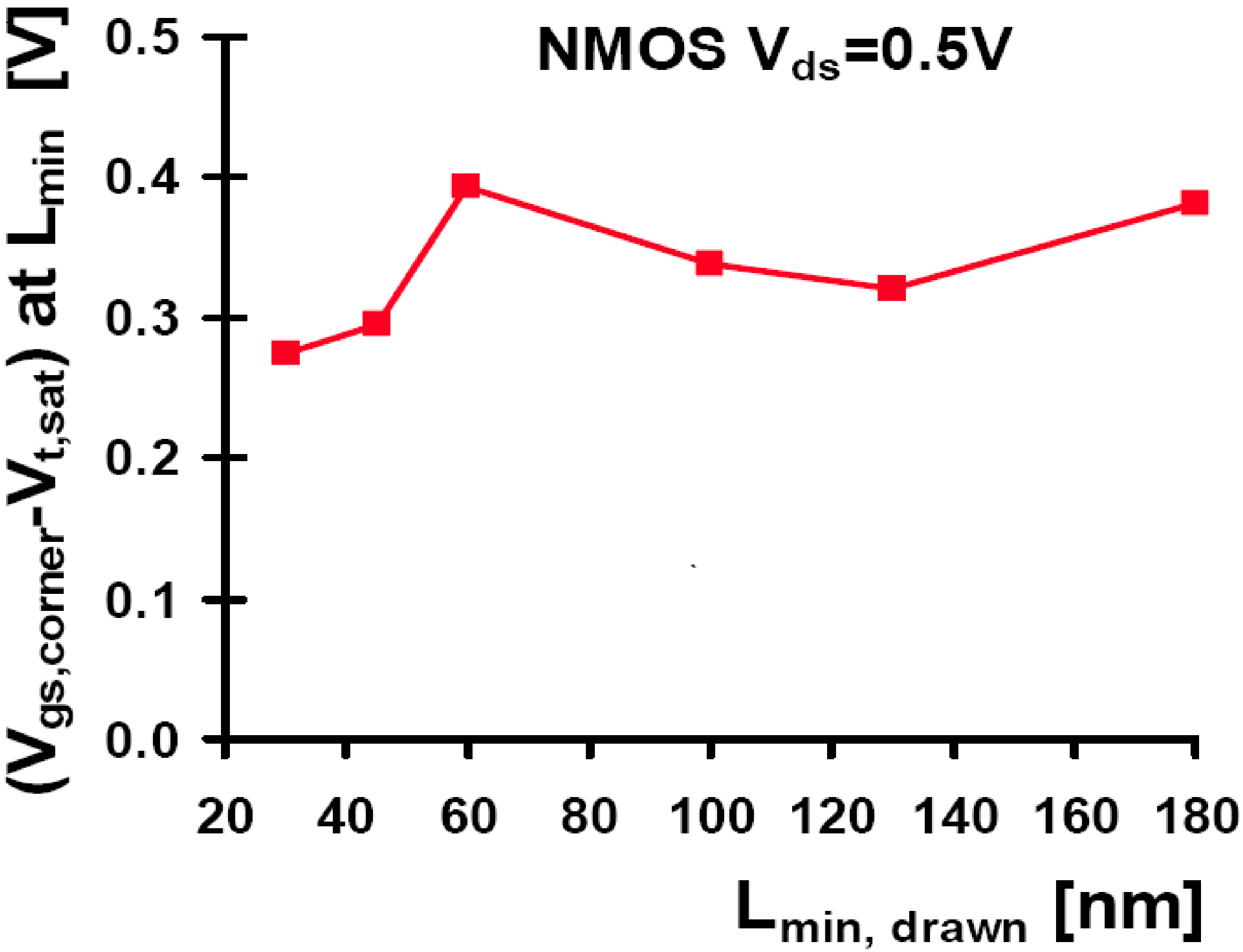
[Vertregt, IEDM'06]

Not so very much of a change…..



[Vertregt, IEDM'06]

“square law” region remains around 300mV



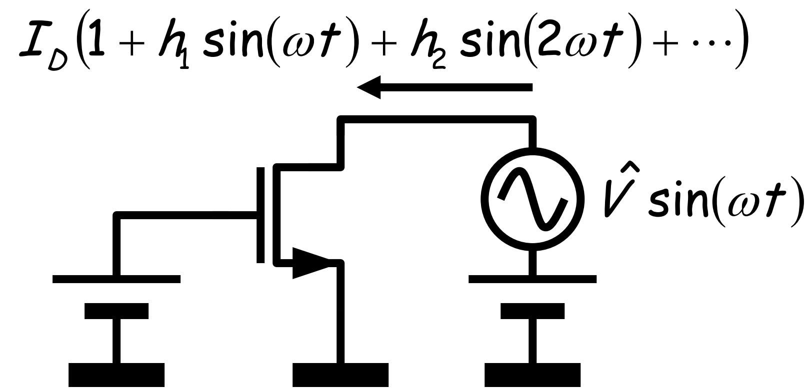
[Vertregt, IEDM’06]

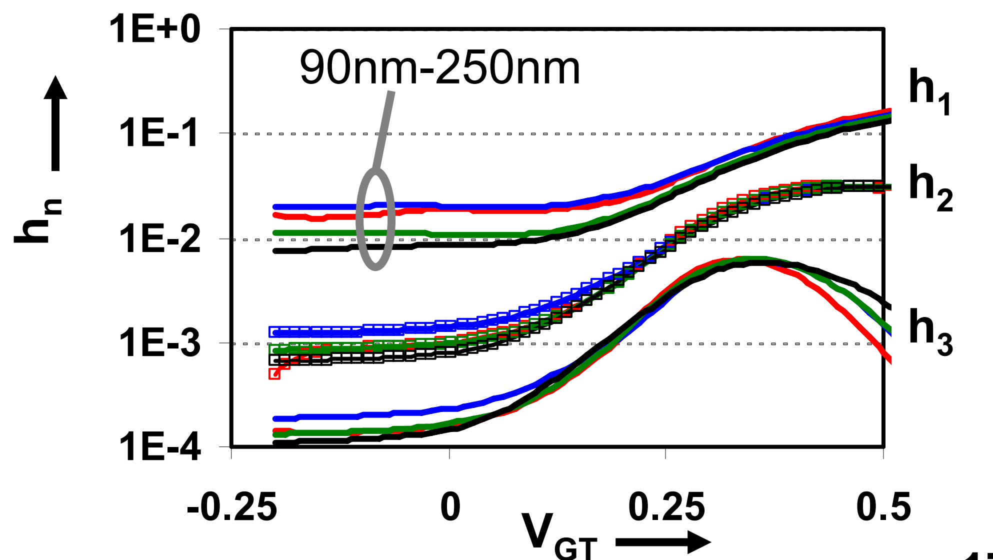
Output conductance

Quasi-DC distortion:

- **<u>fixed</u>** V_{DS} and swing
- vary technology
- keep L=1μm

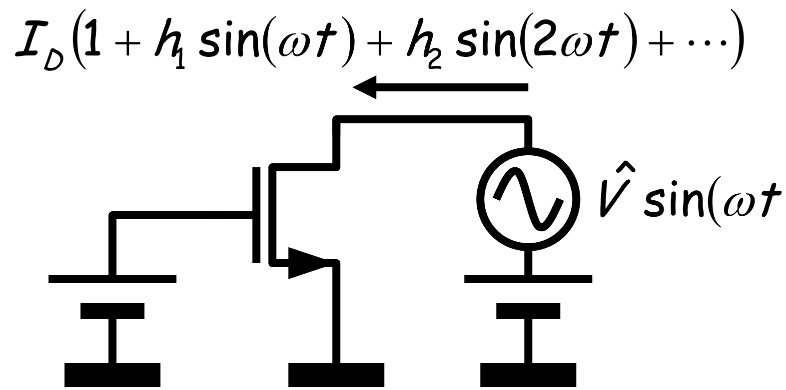
"no" effect technology





Output conductance

Quasi-DC distortion:



- **<u>vary</u>** V_{DS} and swing
- vary technology
- keep L=1μm

- 250nm → 90 nm:
  - – h_2, h_3 x 10
  - – $g_m \cdot r_{out}$ x 1/3

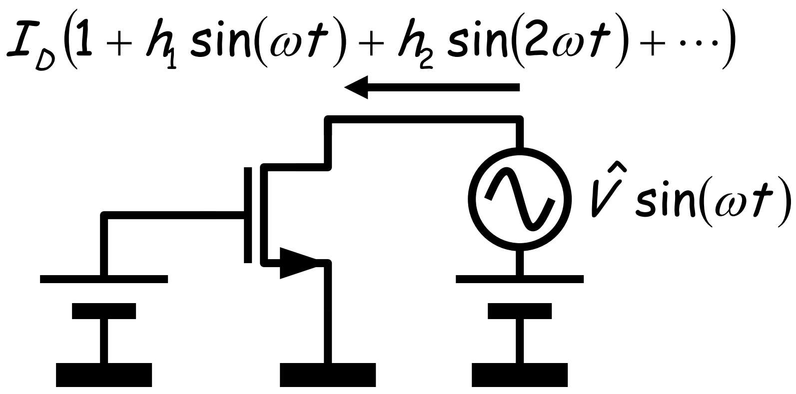
} → - More distortion
- Less loopgain

Output conductance

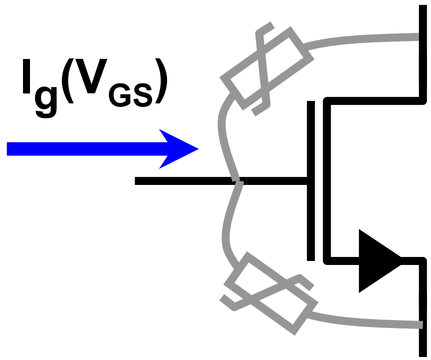
Quasi-DC distortion:

- **<u>vary</u>** V_{DS} and swing
- vary technology
- ~~keep L=1μm~~

- Only guaranteed: $g_m \cdot r_{out} >> 1$



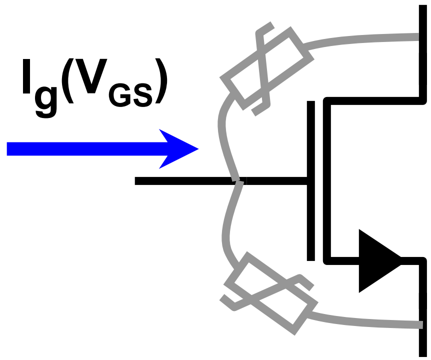
Gate leakage:



Direct tunneling through oxide

- DC input current (bipolar-like)
- dependent on V_{GS}, V_{DS}, W, L, …
- t_{OX} – 0.2nm ⟶ I_G x 10

Gate leakage:



Direct tunneling through oxide

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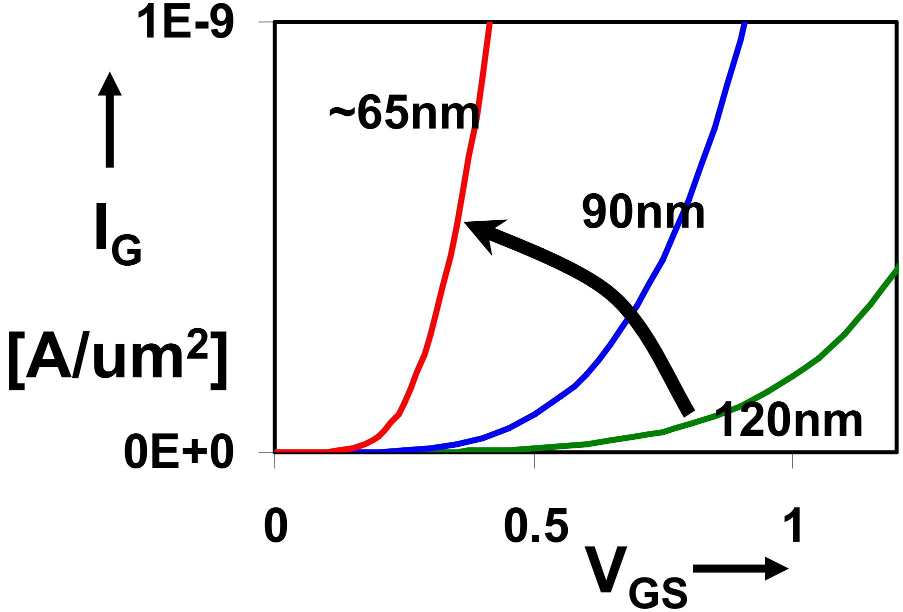
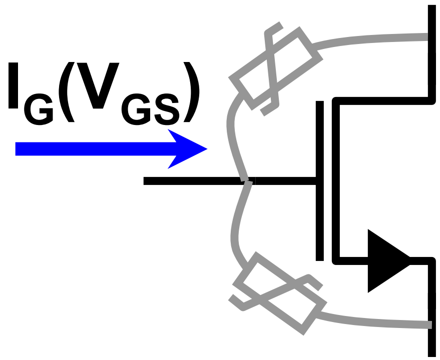
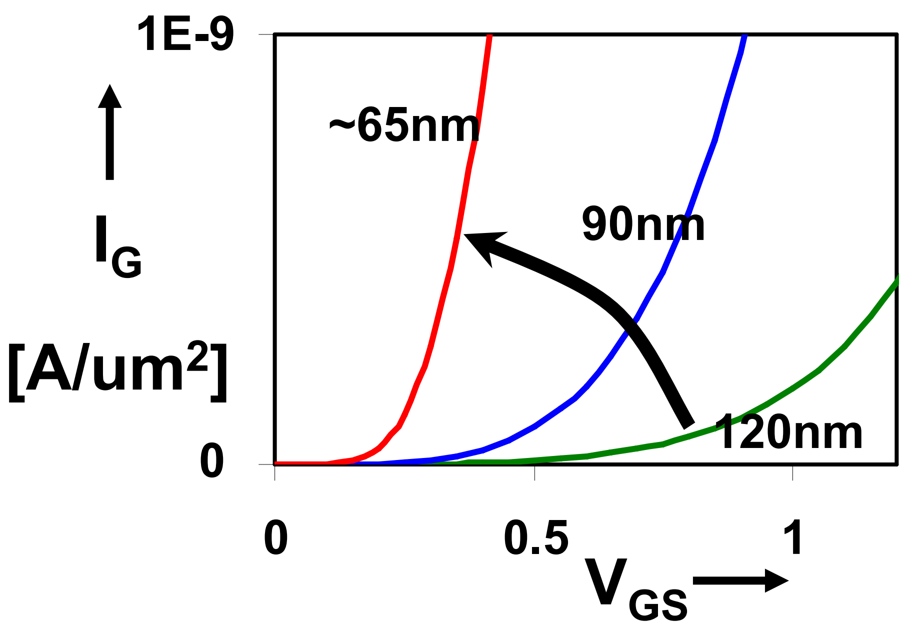


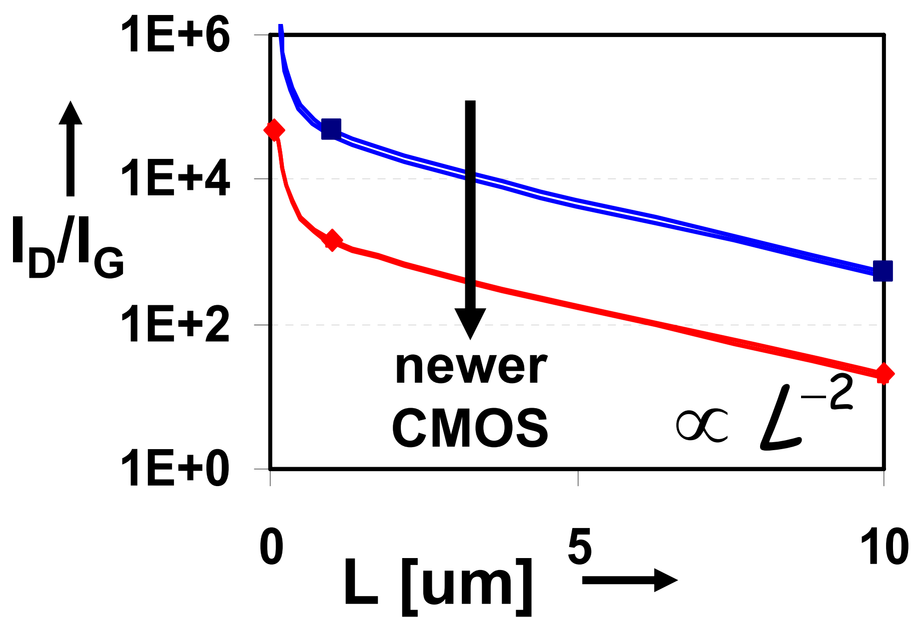
Gate leakage:



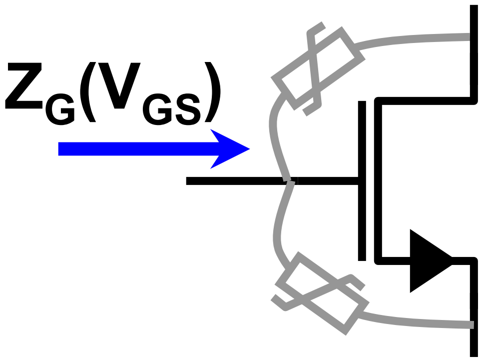
Direct tunneling through oxide

- significant at normal conditions
- DC input current (bipolar-like)
- dependent on V_{GS}, W, L, …





Gate leakage: f_{gate}



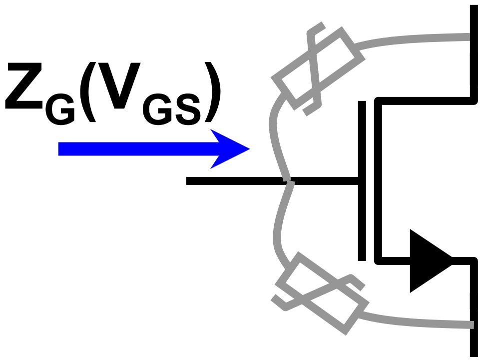
$f < f_{gate} \rightarrow$ resistive Z_G
$f > f_{gate} \rightarrow$ capacitive Z_G

$$\boxed{f_{gate}(V_{DS}, V_{GS}) = \frac{1}{2\pi\, c_{in}\, r_{tunnel}}}$$

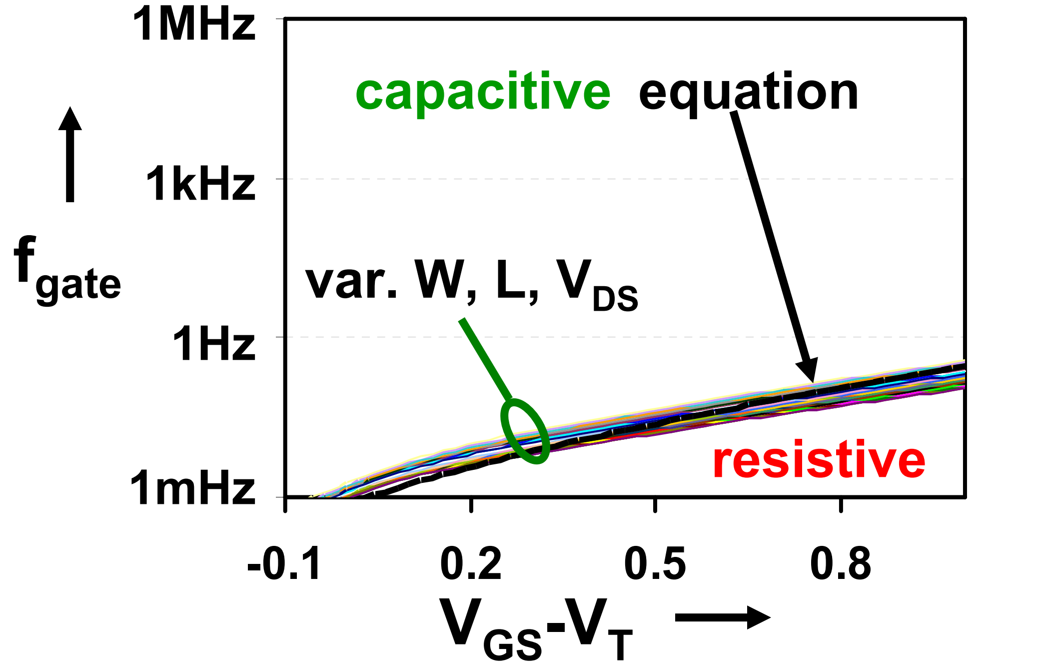
$$\cong 1.5 \cdot 10^{16} \cdot V_{GS}^{2}\, e^{tox(V_{GS}-13.6)} \qquad t_{ox}\,[nm]$$

f_{gate} = area independent
≈ V_{DS} independent

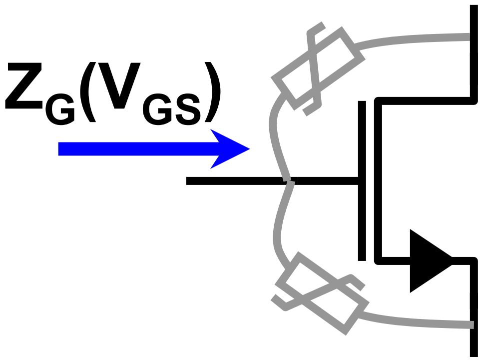
Gate leakage: f_{gate}

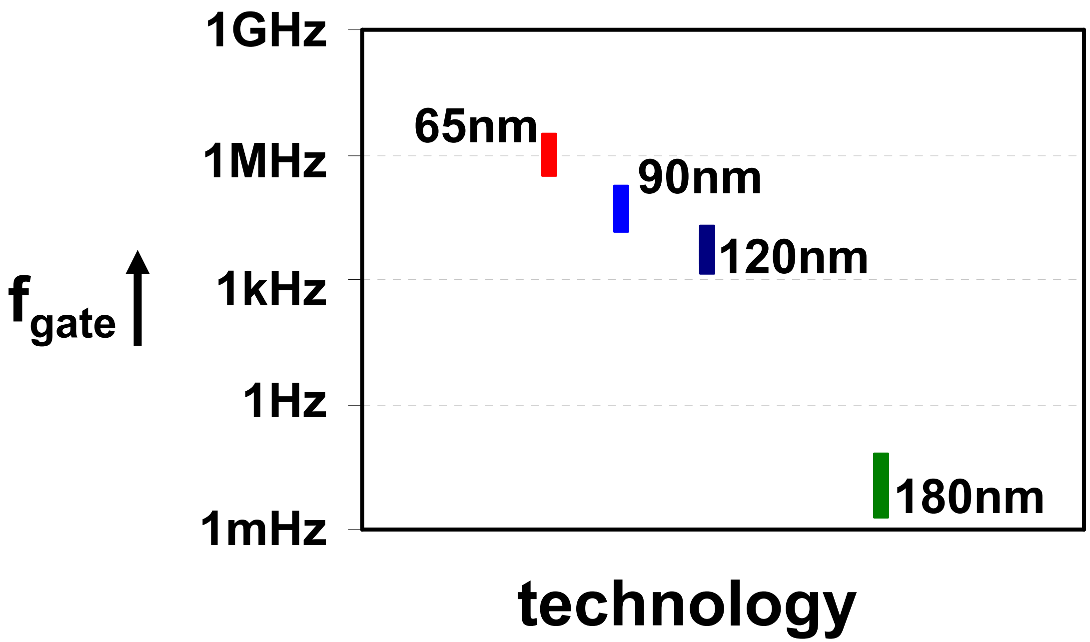


180nm technology: f_{gate} < 0.1Hz



Gate leakage: f_{gate}





Gate leakage: matching

spread due to V_T-spread only

- $$\frac{\sigma_{ID}^2}{I_D^2} = \left(\frac{A_{Vt}}{\sqrt{WL}} \cdot \frac{g_m}{I_D} \right)^2$$

[Pelgrom]

Gate leakage: matching

spread due to V_T-spread and I_G-spread

- $$\frac{\sigma_{ID}^2}{I_D^2} = \left(\frac{A_{VT}}{\sqrt{WL}} \cdot \frac{g_m}{I_D} \right)^2 + \left(\frac{\zeta \cdot f_{gate} \cdot L^2}{\sqrt{WL}} \right)^2$$

Gate leakage: matching

spread due to V_T-spread and I_G-spread

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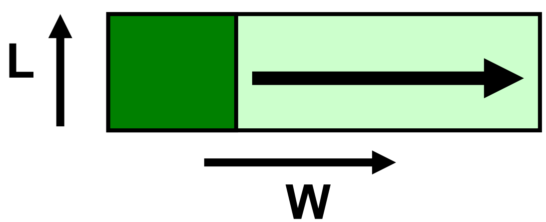
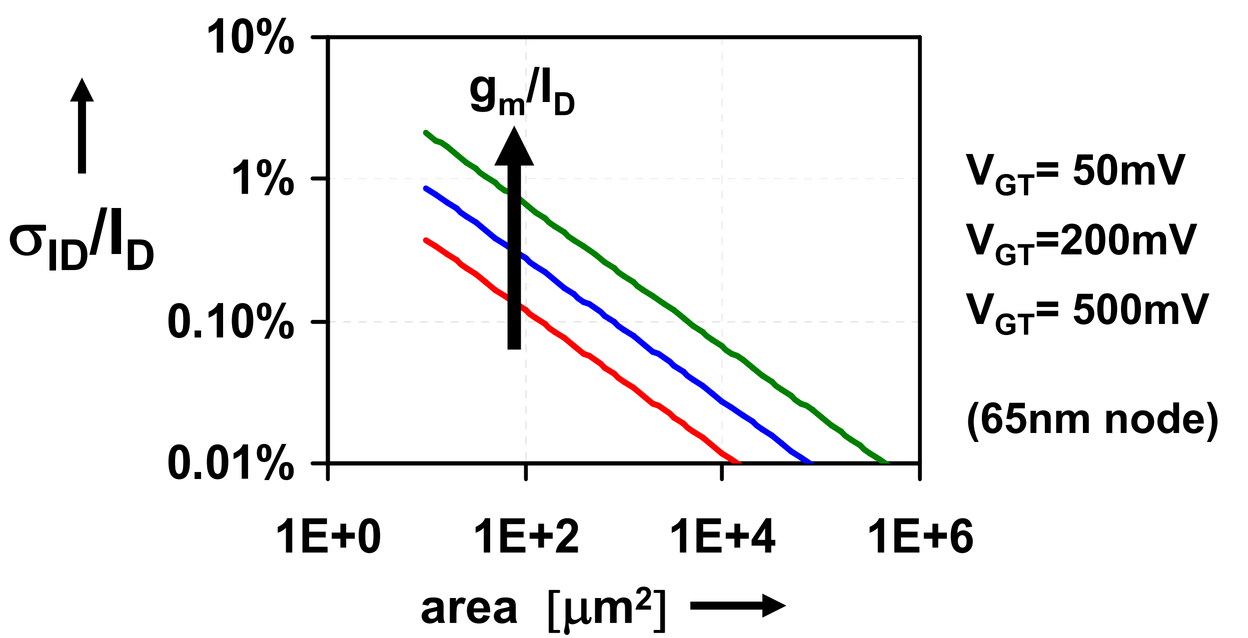


L = constant!



Gate leakage: matching

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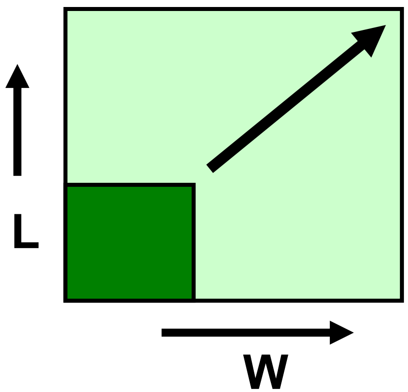
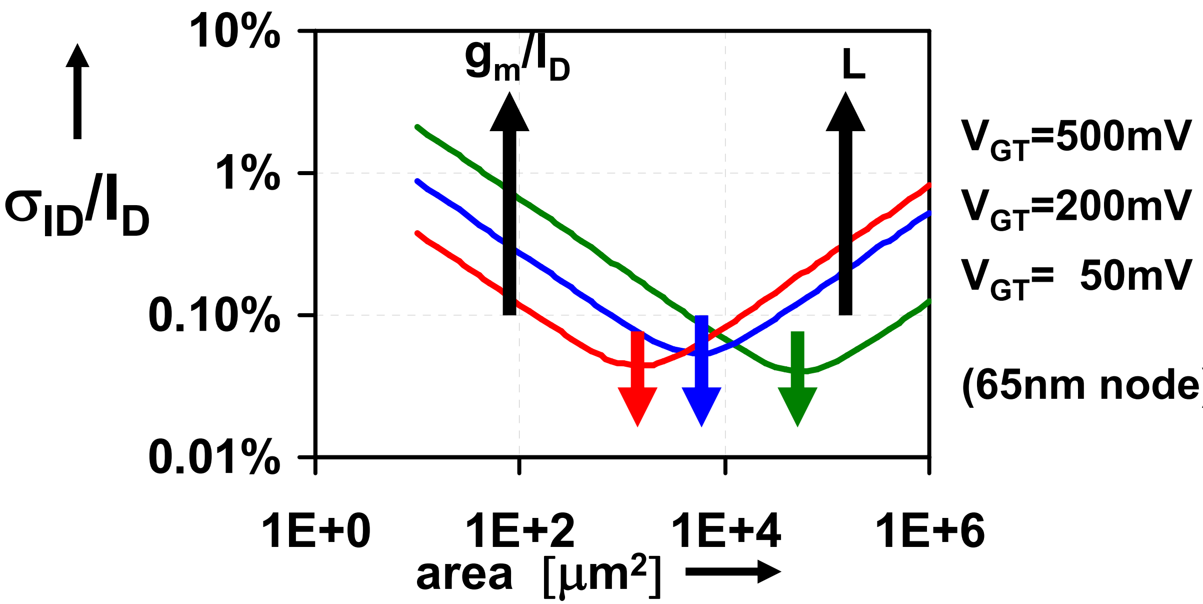


L increases!



Gate leakage

- spread due to V_T-spread and I_G-spread

$$\frac{\sigma_{ID}^2}{I_D^2} = \left(\frac{A_{VT}}{\sqrt{WL}} \cdot \frac{g_m}{I_D} \right)^2 + \left(\frac{\zeta \cdot f_{gate} \cdot L^2}{\sqrt{WL}} \right)^2$$

newer CMOS:
- A_{VT} hardly decreases
- f_{gate} increases
- mind the L!

- gate shotnoise: $i_g^2 = 2qI_G$

Summary: technology

- Classical analog circuits not trivial:
  - Output conductance nonlinearity
  - Gate leakage issues
  - Low voltage operation

references

- Annema, A.J., Nauta, B., Langevelde, R van , Tuinhout, H "Analog Circuits in Ultra-Deep Sub-Micron CMOS" IEEE J. Solid State Circuits, January 2005

- Maarten Vertregt, “The analog challenge of nanometer CMOS” Plenary talk IEDM, December 2006

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  - **Noise canceling**
  - 1/f noise reduction
  - Distortion canceling
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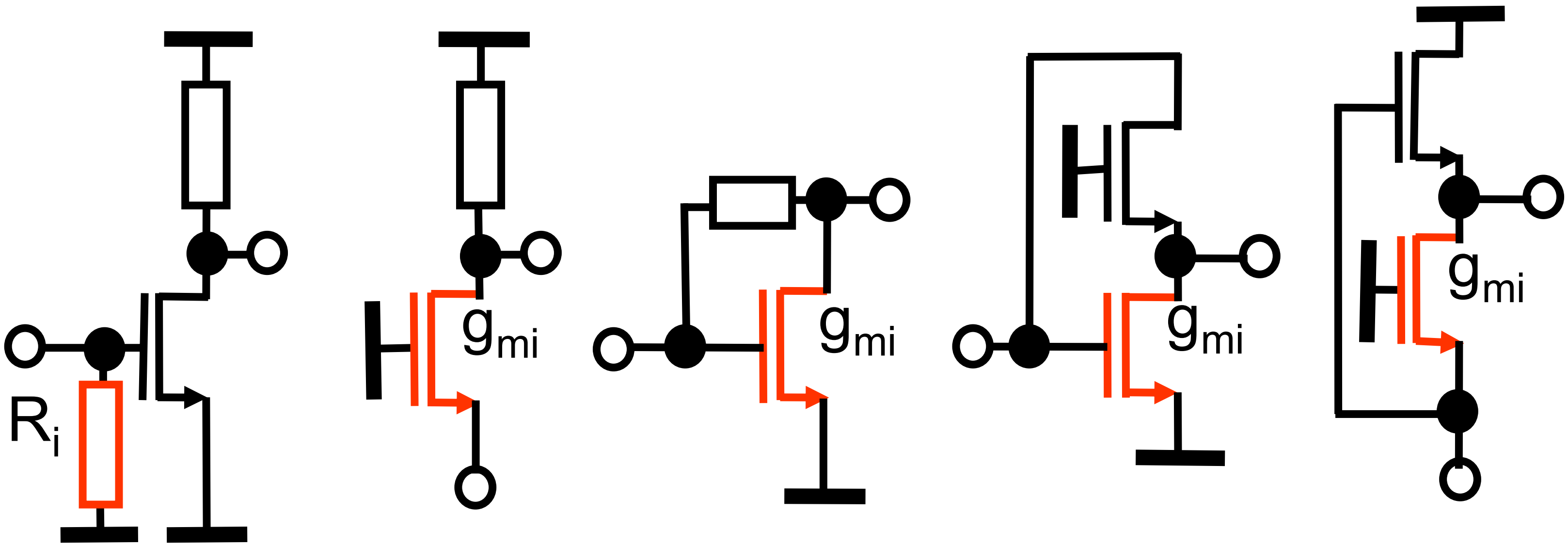
Noise canceling technique

- For LNAs
  - with matched impedance input
  - with (ultra!) wide bandwidth

- Alternative for feedback techniques

Conventional Wideband Techniques: (1)



- Input device determines $F = SNR_{OUT}/SNR_{IN}$

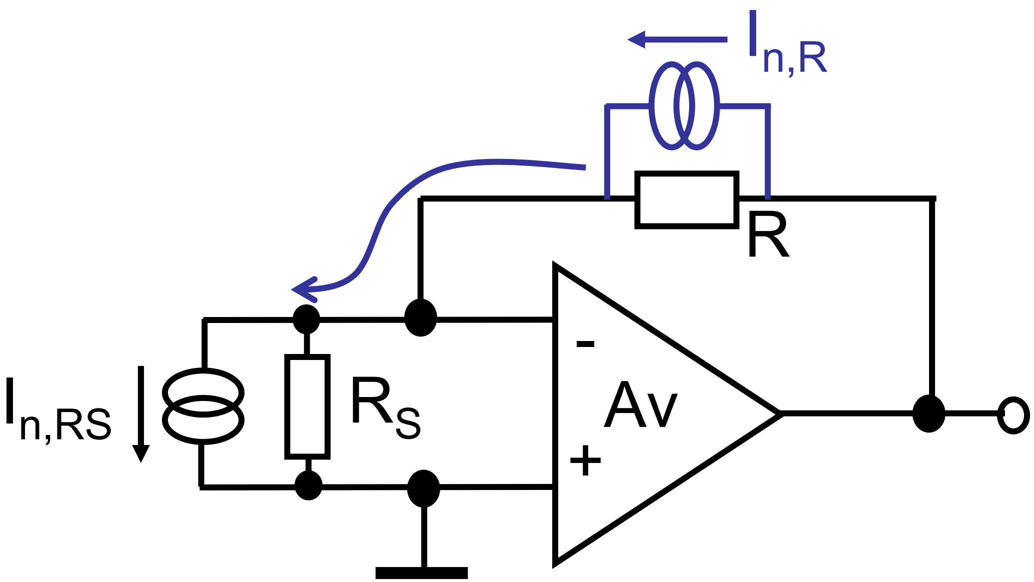
- F to $Z_{IN}=R_S$ Trade-off:

  Low F ➡ *Laaaaaarge* g_{mi} and R_i

  $Z_{IN}=R_S$ ➡ $g_{mi}=1/R_S$ and $R_i=R_S$ ➡ F>2 (NF>3dB)!!

Existing Wideband Techniques: (2)

- F to $Z_{IN}=R_S$ *de*coupling via feedback



$$F = 1 + \frac{\overline{I_{n,R}^2}}{\overline{I_{n,RS}^2}} = 1 + \frac{R_S}{R}$$

$$R_{IN} = \frac{R}{1+Av} = R_S$$

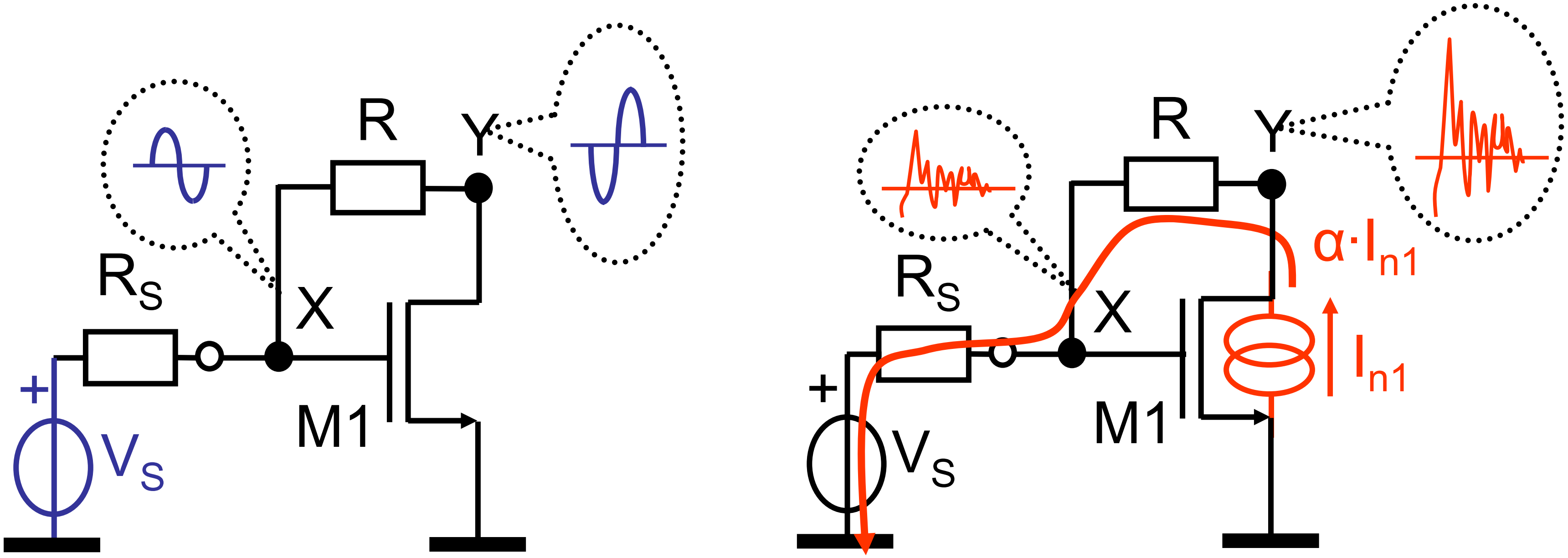
$$F = 1 + \frac{1}{1+Av}$$

☹ Av=Multiple stages ⇨ Instability!

☹ Matching and Gain coupled ⇨ AGC@$Z_{IN}=R_S$!

☹ Loop-gain <1 for ∀ Av ⇨ Modest Linearity!

Noise Canceling Technique: Principle (1)

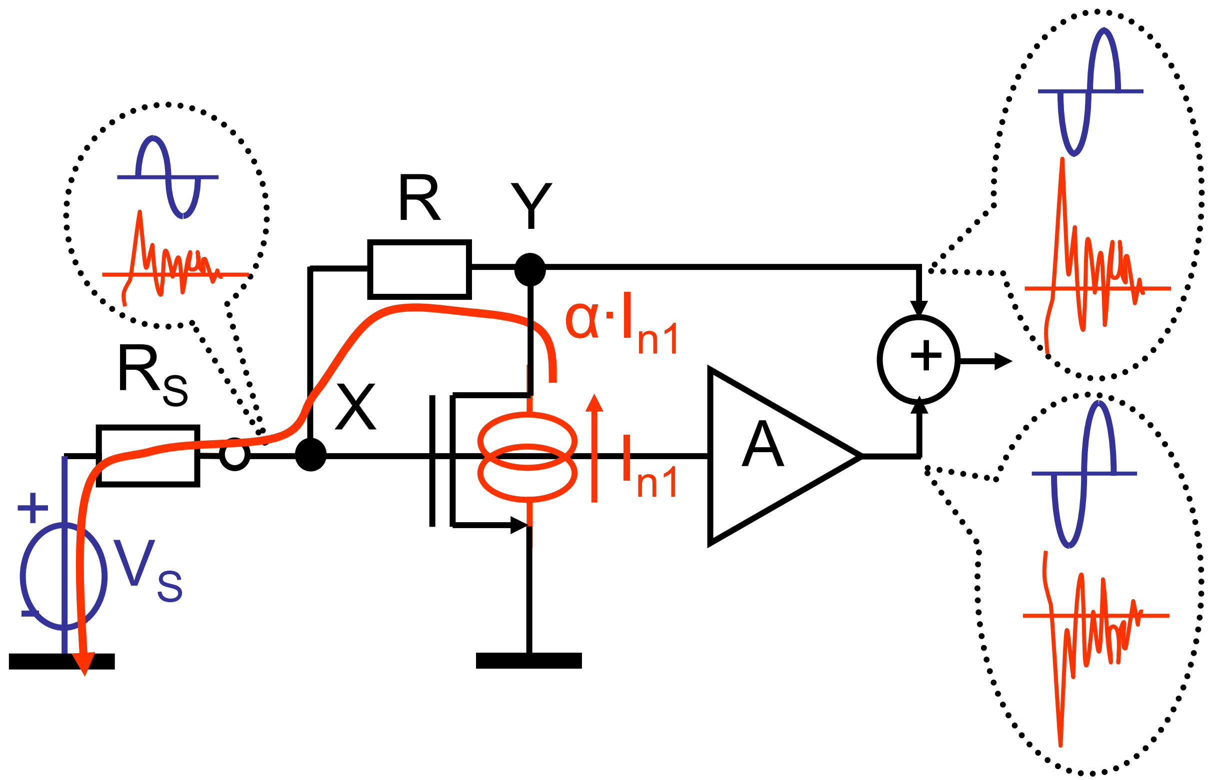


$$R_{IN} = \frac{1}{gm_1}$$

✓Signals @ nodes X and Y: OPPOSITE SIGN

✓Noise @ nodes X and Y : EQUAL SIGN!

Noise Canceling Technique: Principle (2)



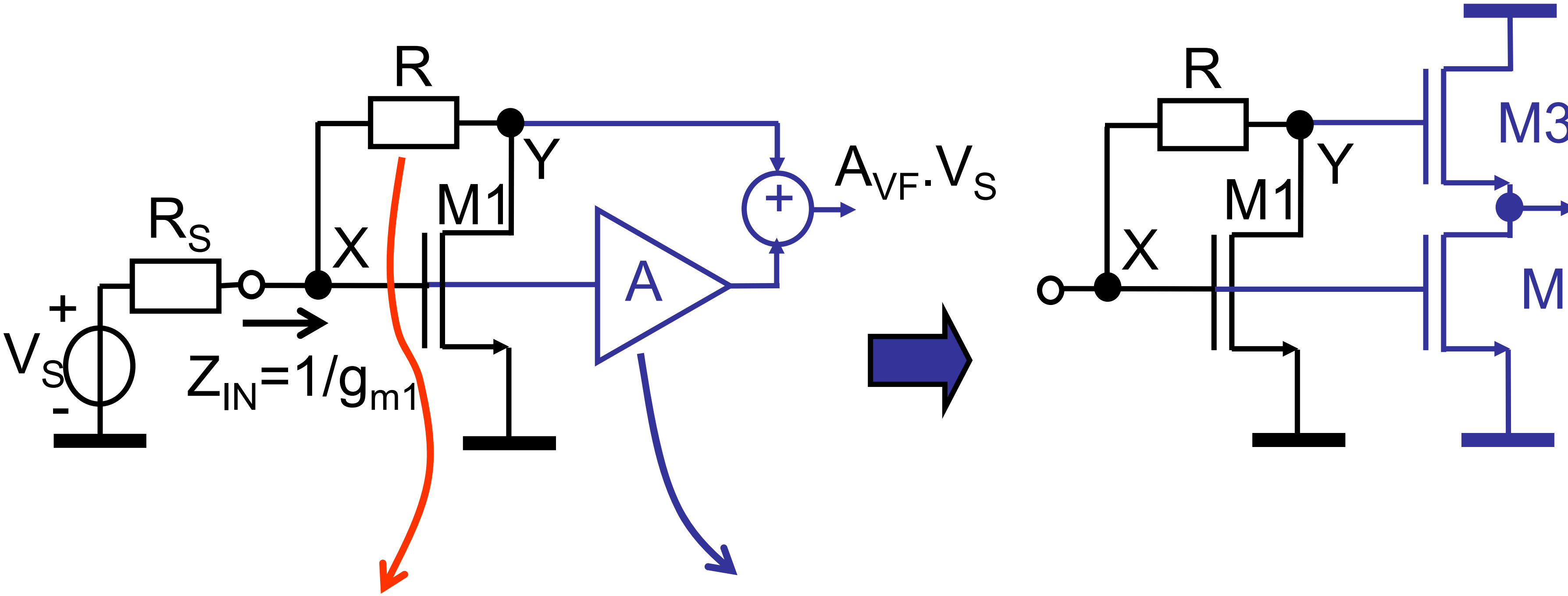
☺ Noise Cancels if $V_{nX}A + V_{nY} = 0$ ➡ $A = -(1 + R/R_S)$

☺ But Signals Add !!

Matching, …but no output noise ➡ R_{IN} and F *de*coupled

[Bruccoleri, et al.ISSCC92]

Noise Canceling Technique: Properties (1)

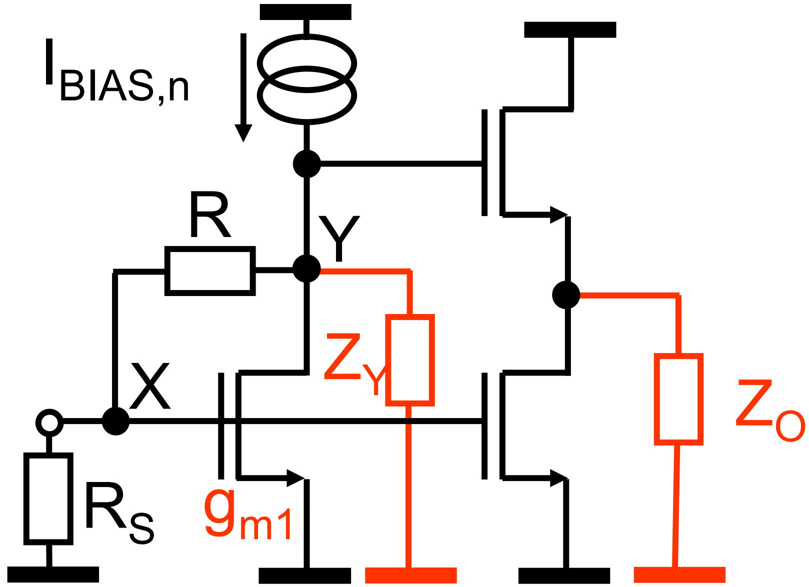


☺ $F = 1 - \frac{2}{A_{VF}} + \frac{NEF}{g_{m2}R_S} \cdot \frac{8 - 6 \cdot A_{VF} + A_{VF}^2}{A_{VF}^2} > 1 - \frac{2}{A_{VF}}$

☺ Feed-forward ➡ Instability risks relaxed

☺ Matching and Gain decoupled ➡ AGC @ $R_{IN}=R_S$!

Noise Canceling Technique: Properties (2)



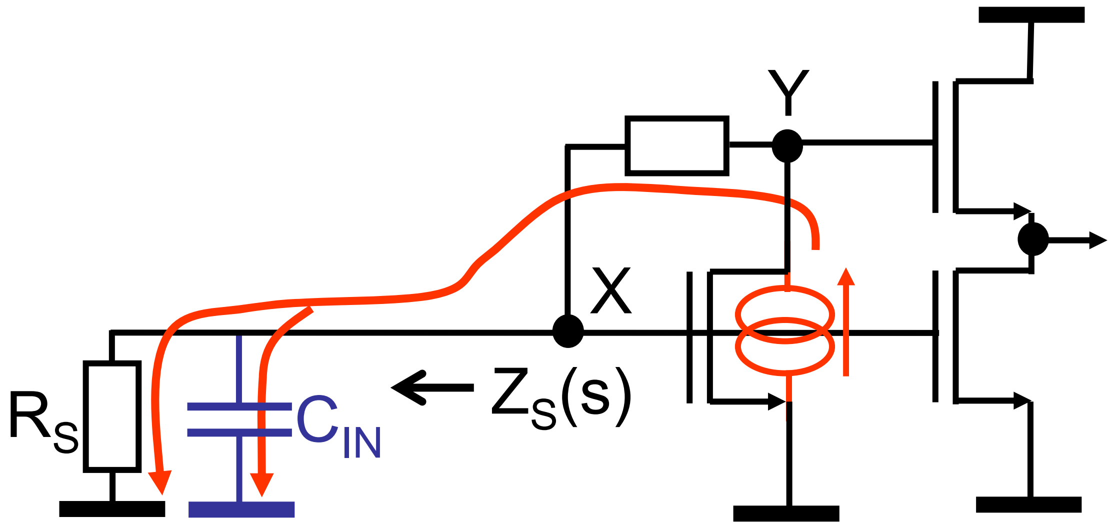
- Bias noise $I_{BIAS,n}$ cancels too
- Robust to device parameter variations:

☺ Canceling independent of: Z_Y, Z_O, $Z_{IN}=1/g_{m1}$

☺ For $\varepsilon=|g_{m2}/g_{m3}-1-R/R_S|$ ⇒ $F=1+NEF\cdot(\varepsilon/A_{VF})^2$

(Monte Carlo: $4\cdot\sigma(NF) < 0.2$dB @2GHz)

Noise Canceling Technique: HF Limitations

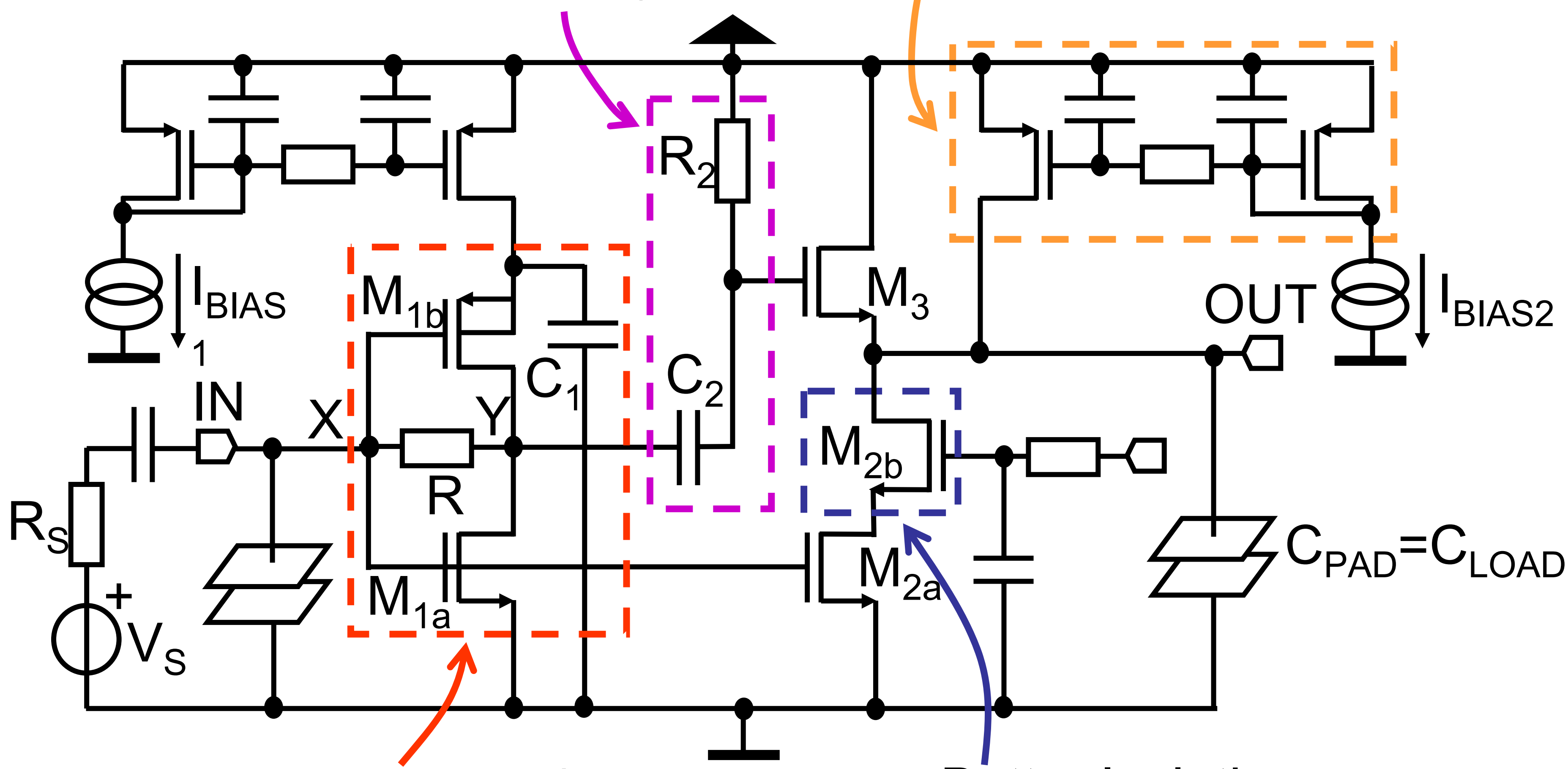


- C_{IN} ➡ Noise canceling degrades @ HF

ΔNF(f) = 0.1dB@ 1GHz and 0.4dB @2GHz (Simulation)

- Compensation helps e.g. shunt peaking

CMOS Circuit Implementation: Schematic

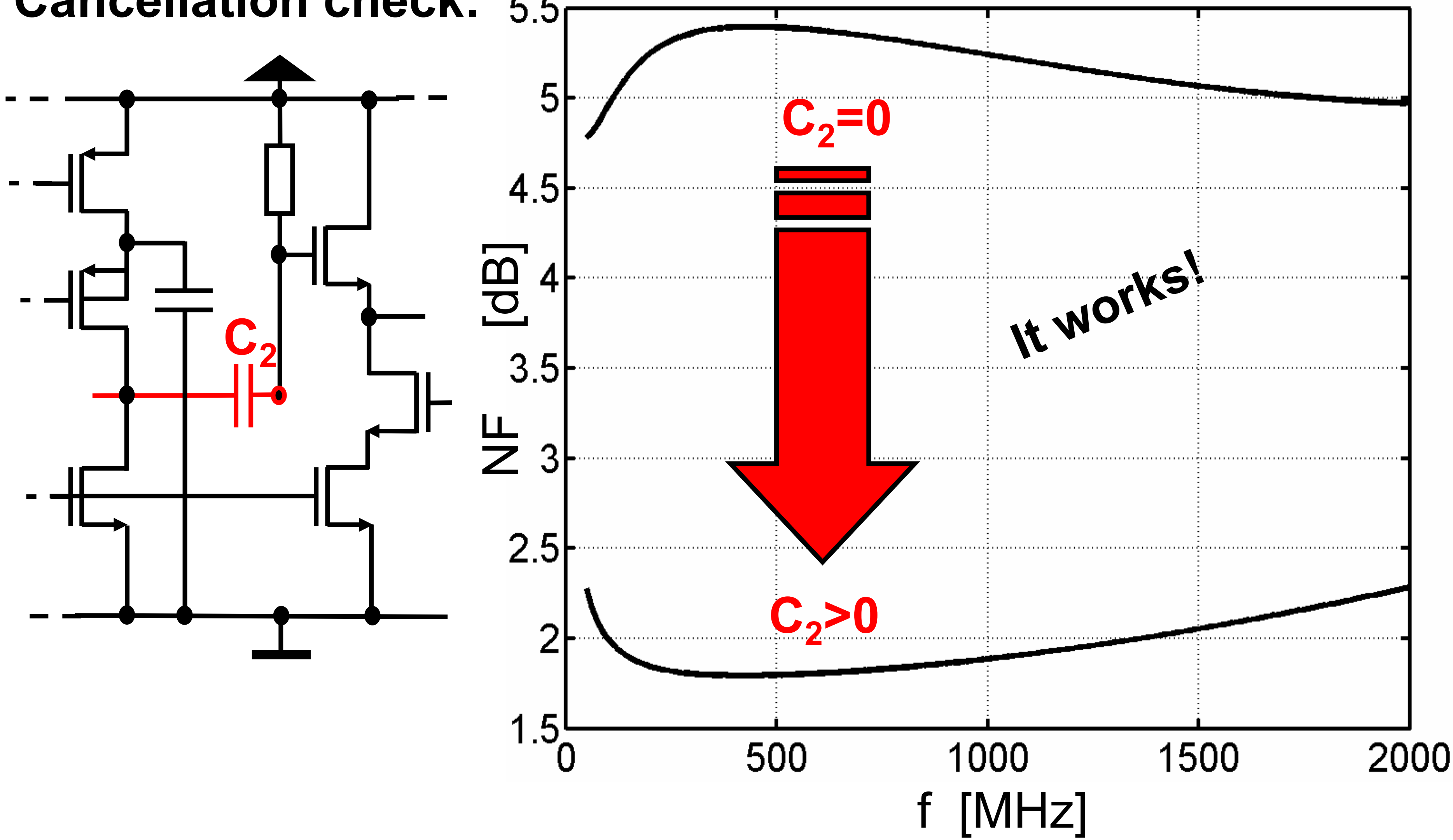


Inverter: Larger g_m/I_D

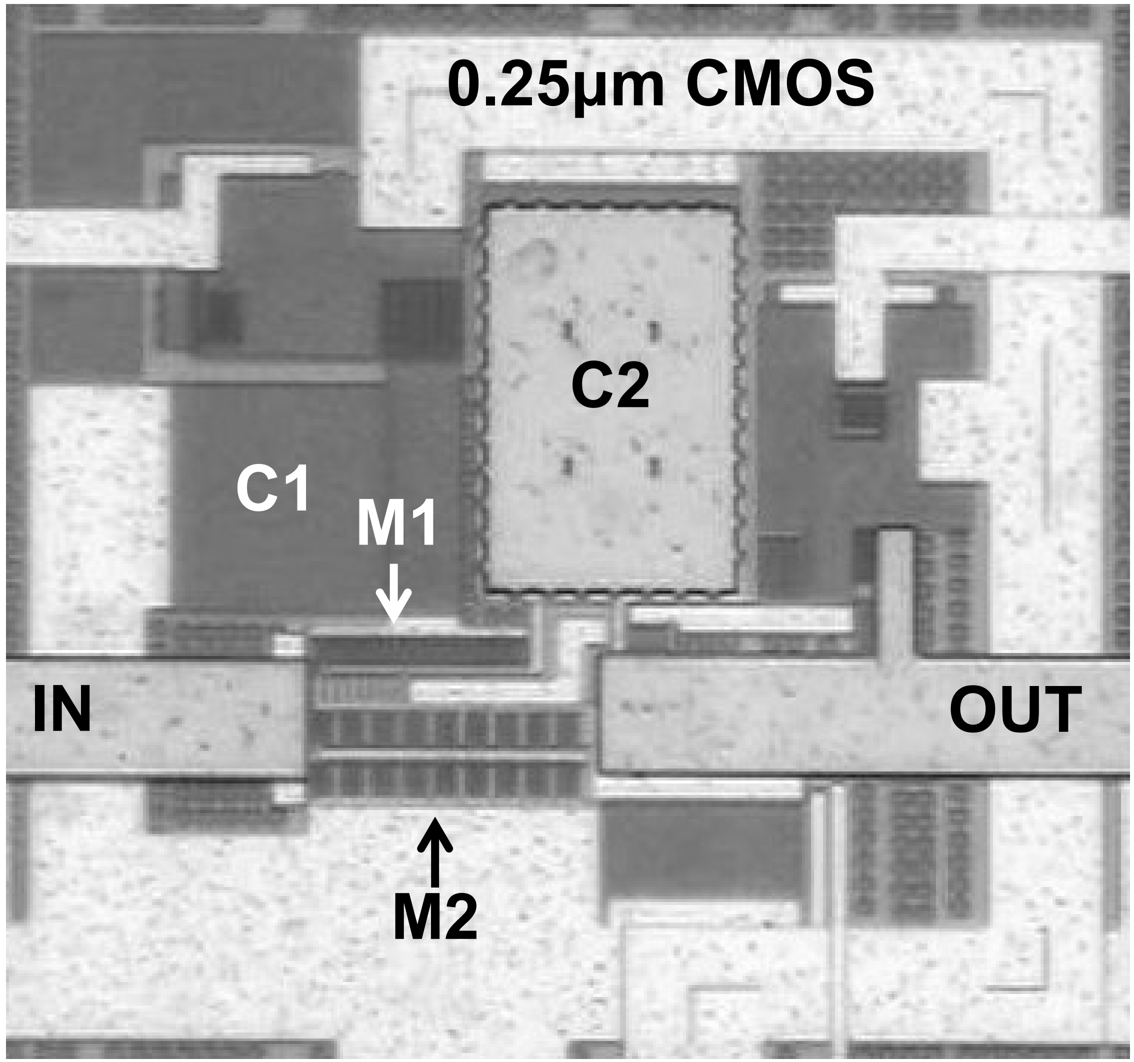
- Better Isolation
- Lower C_{IN}

CMOS Circuit Implementation: Simulation

Cancellation check:



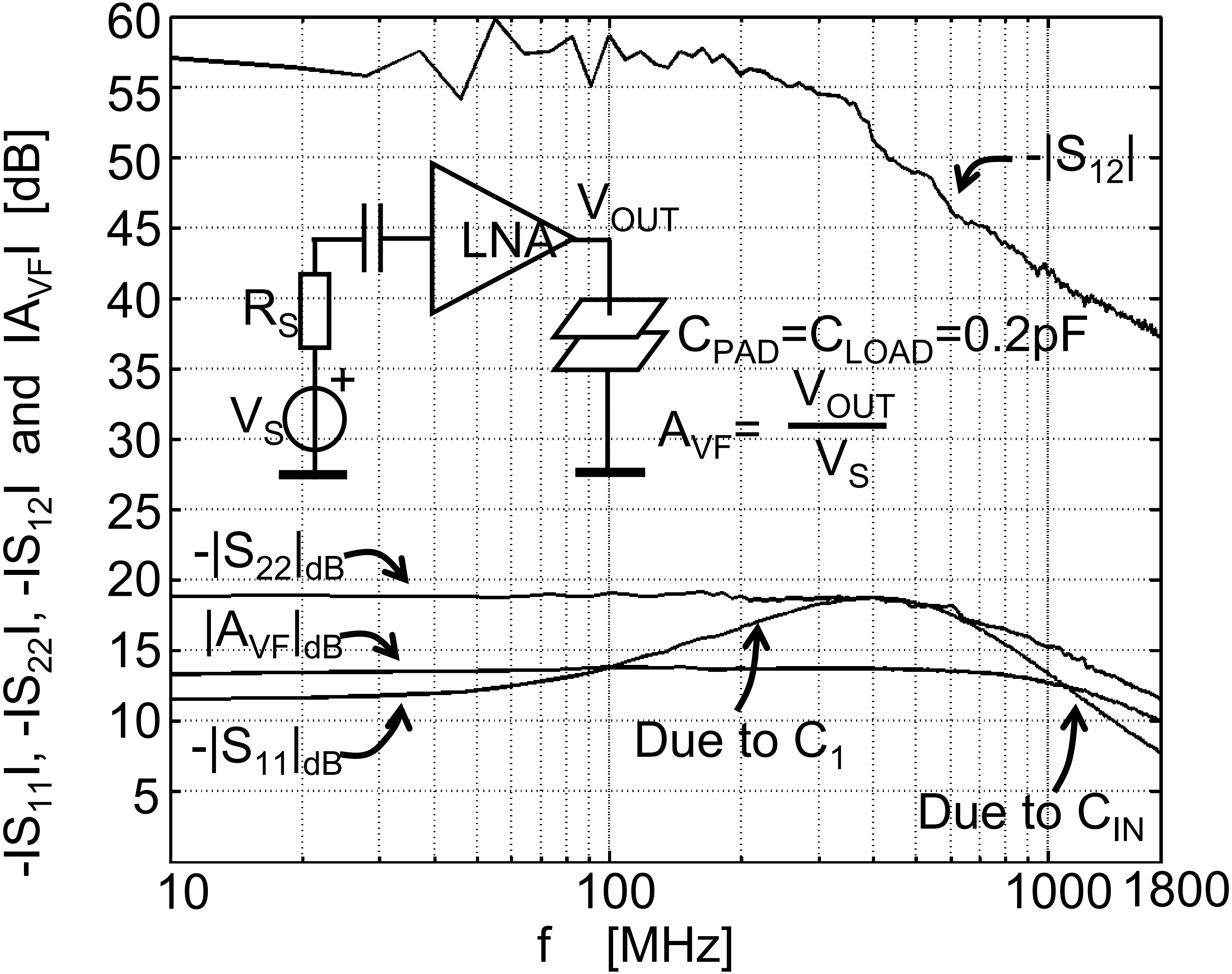
CMOS Circuit Implementation: Chip



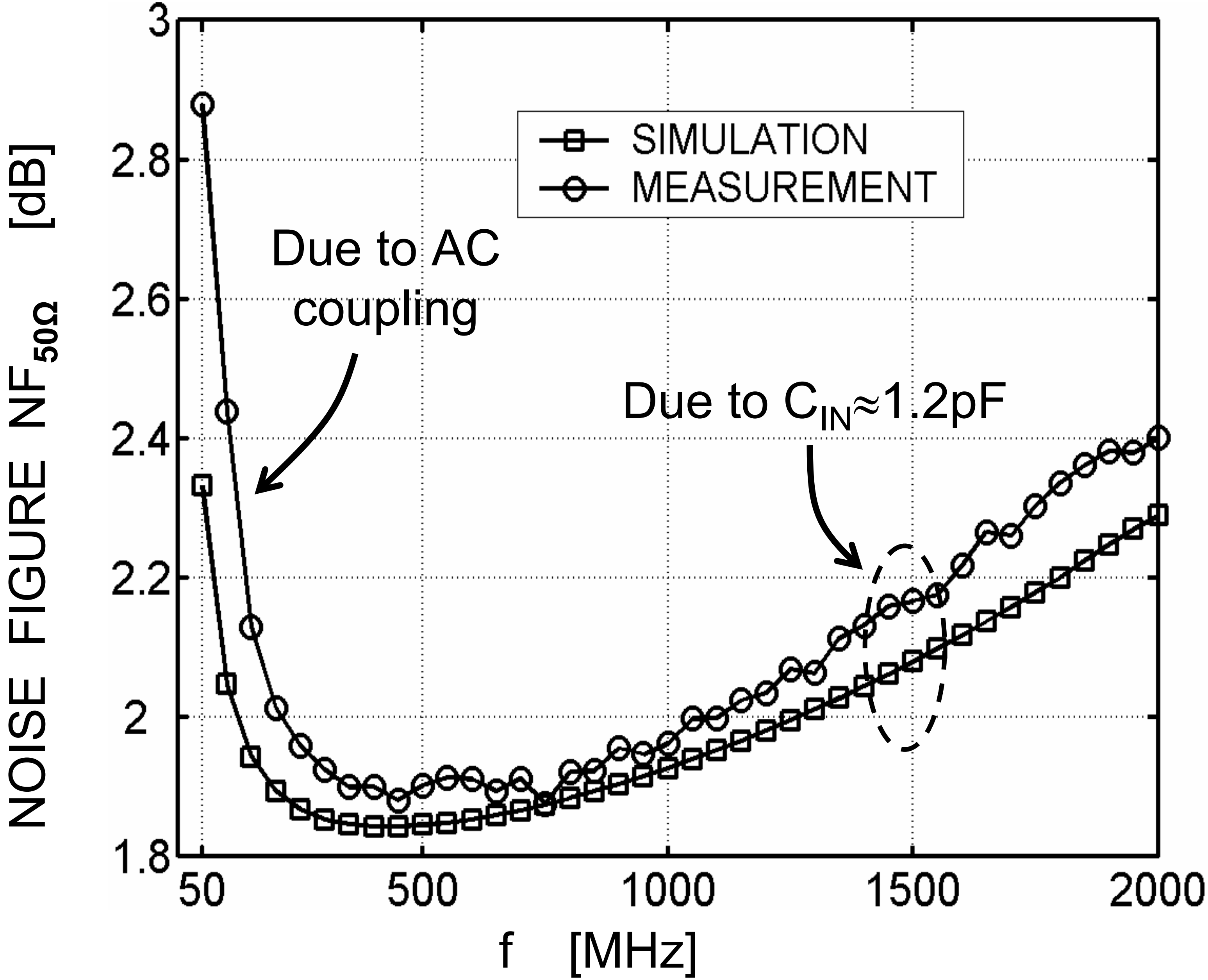
0.25 mm

0.3 mm

Measurement Results: (On-Wafer)



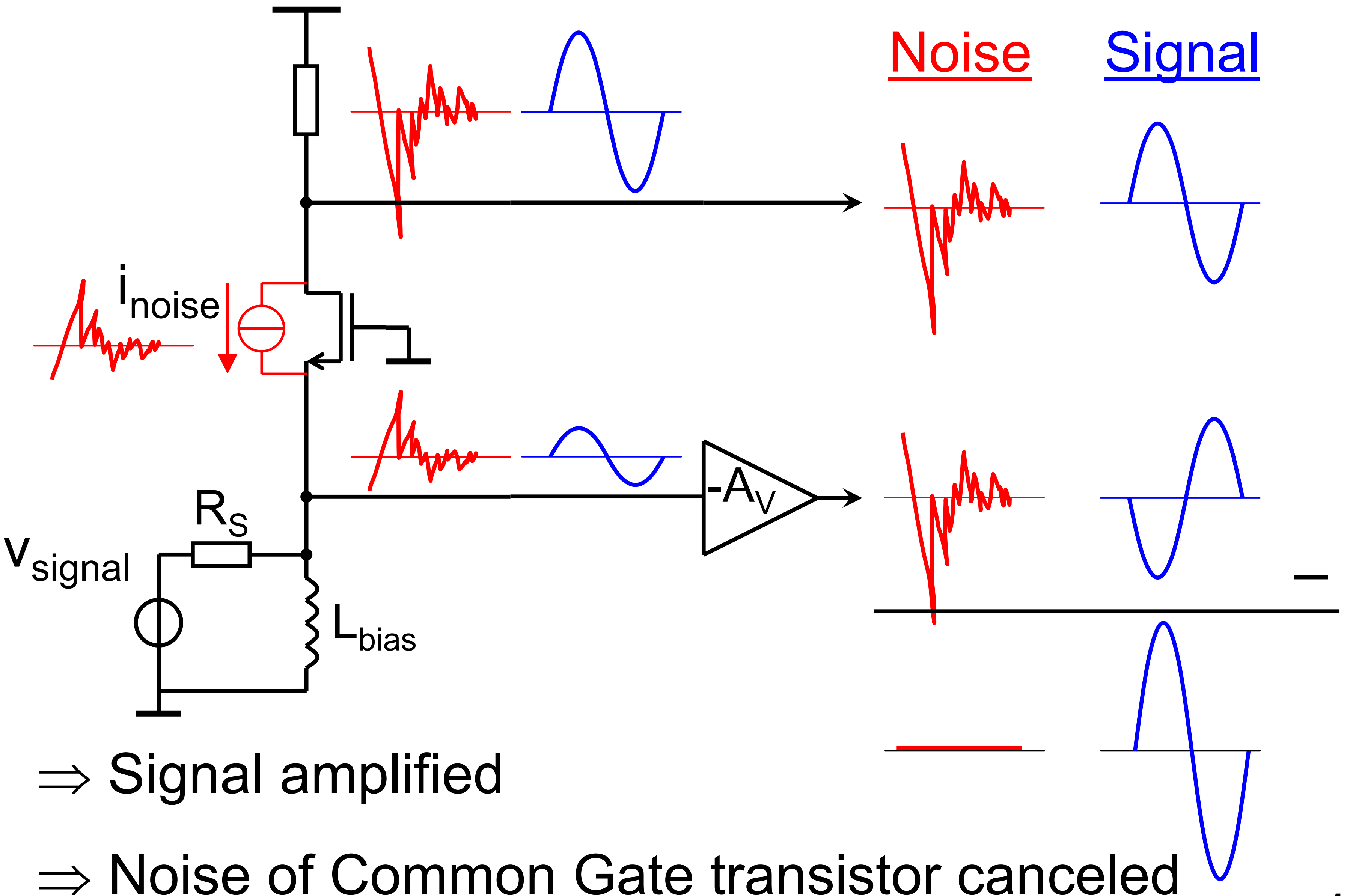
Measurement Results: NF (PCB)



Measurement Results: Summary

PROPERTY	VALUE
$\lvert A_{VF}=V_{OUT}/V_S \rvert$	13.7 dB
-3dB BW	2-1600 MHz ($C_{LOAD}=C_{PAD}=0.2pF$)
$\lvert S_{12} \rvert$	<-36dB in 10-1800 MHz
$\lvert S_{11} \rvert$	<-8dB in 10-1800 MHz
$\lvert S_{22} \rvert$	<-12dB in 10-1800 MHz
IIP3 (input ref.)	0 dBm (f_1=900MHz & f_2=905MHz)
IIP2 (input ref.)	12 dBm (f_1=200MHz & f_2=300MHz)
ICP1 (input ref.)	-9 dBm (f_1=900 MHz)
$NF_{50\Omega}$	≤2dB [0.25-1.1 GHz] & ≤2.4dB [0.15-2 GHz]
$I_{DD}@V_{DD}$	14mA@2.5Volt
Area and Technology	0.3x0.25mm^2 in a 0.25μm CMOS

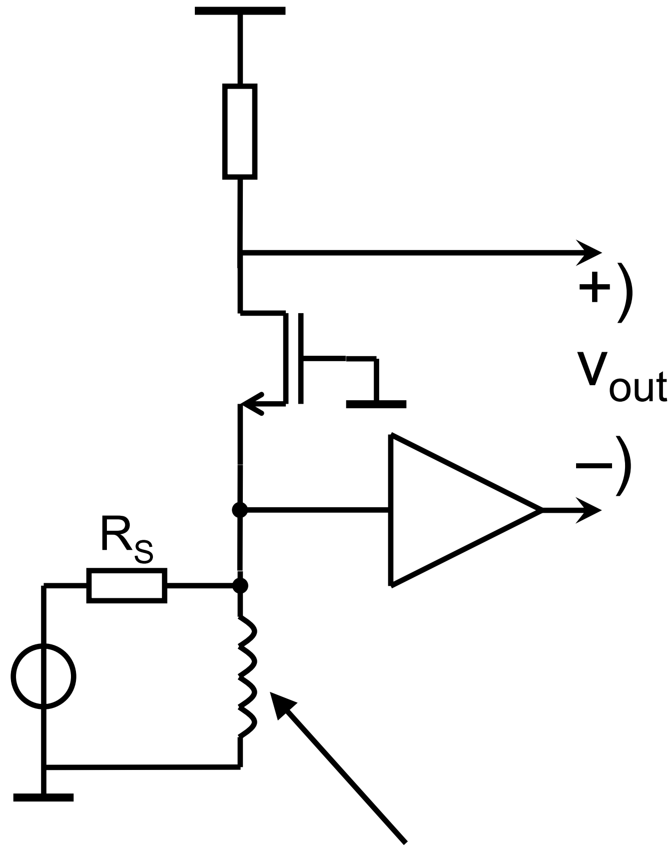
Noise Canceling Technique applied to CG-stage



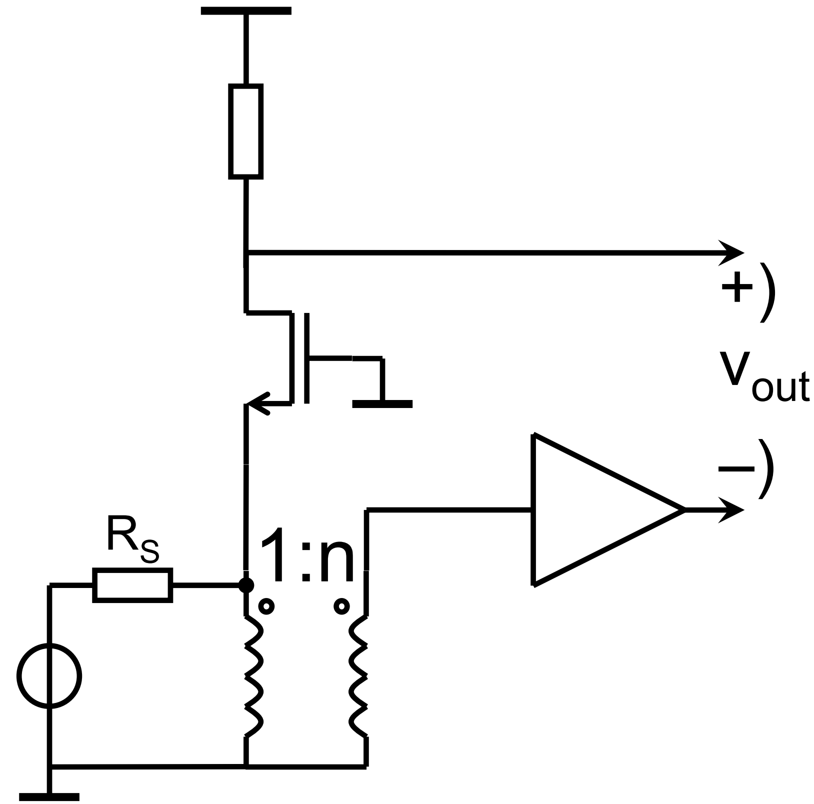
⇒ Signal amplified

⇒ Noise of Common Gate transistor canceled

Implementation A_V using Transformer

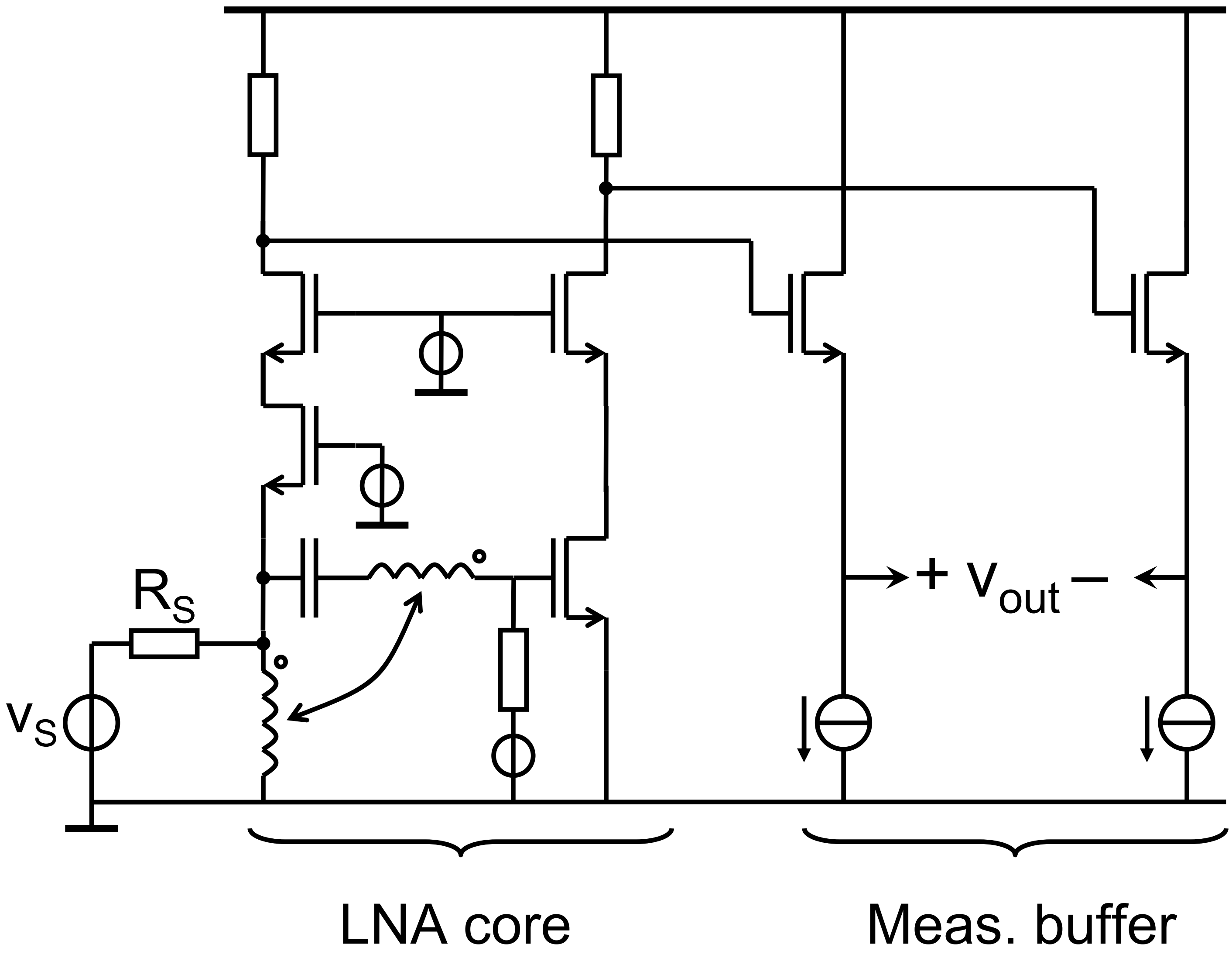


Inductor wanted for
low-noise biasing



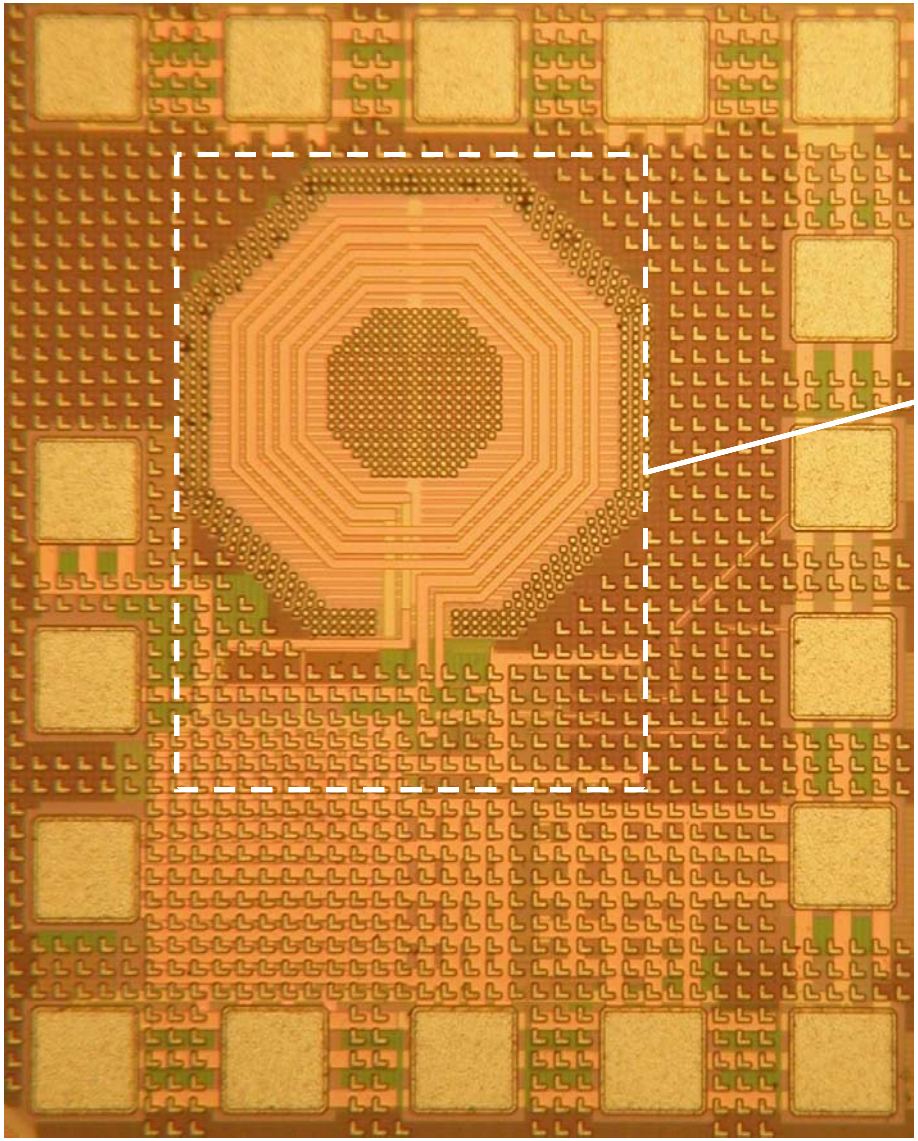
Transformer:
- low noise V-amplification!
- no power dissipation
- minimal area increase

Adding Meas. Buffer (Source-Followers)

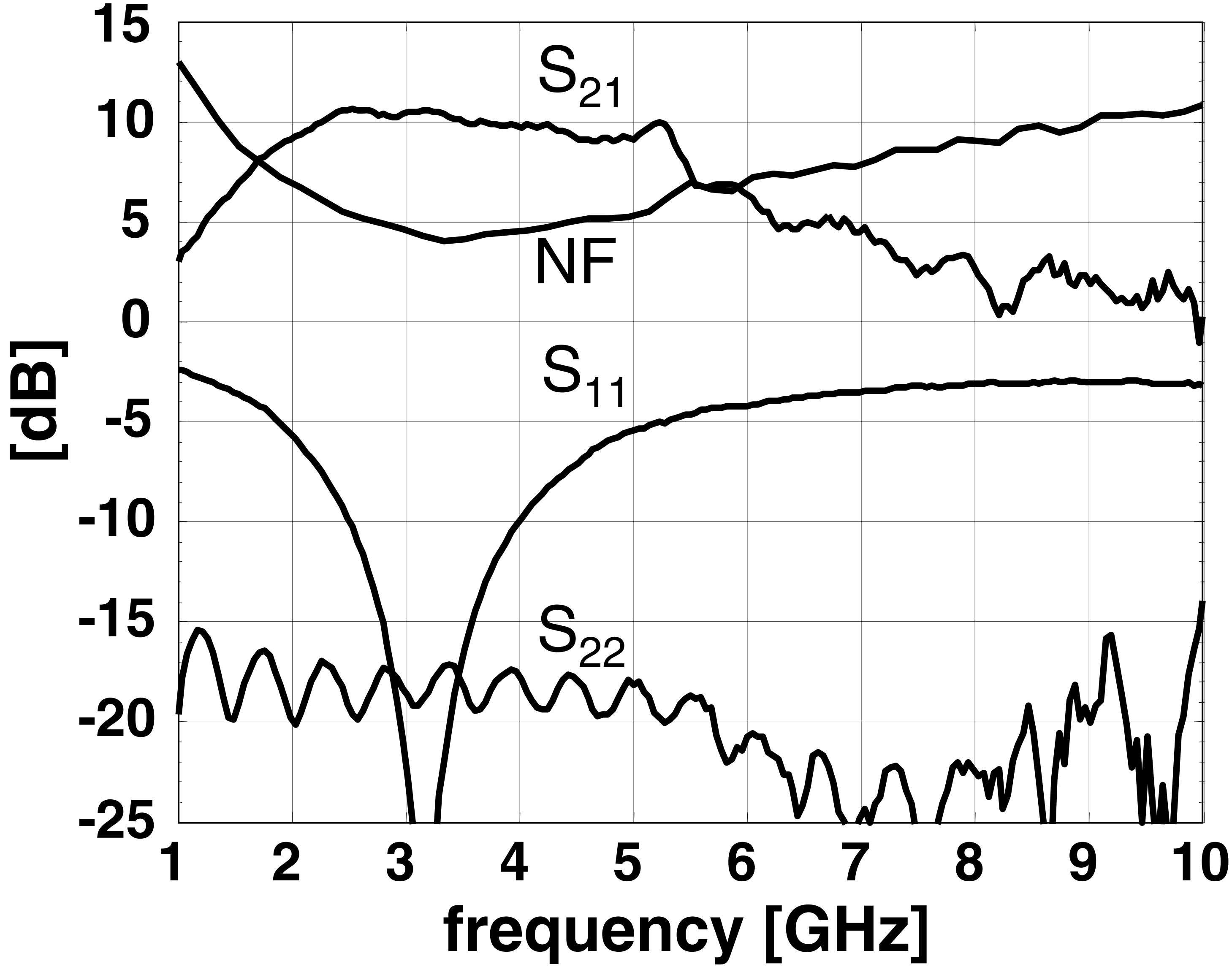


[Blaakmeer et al., RFIC'06]

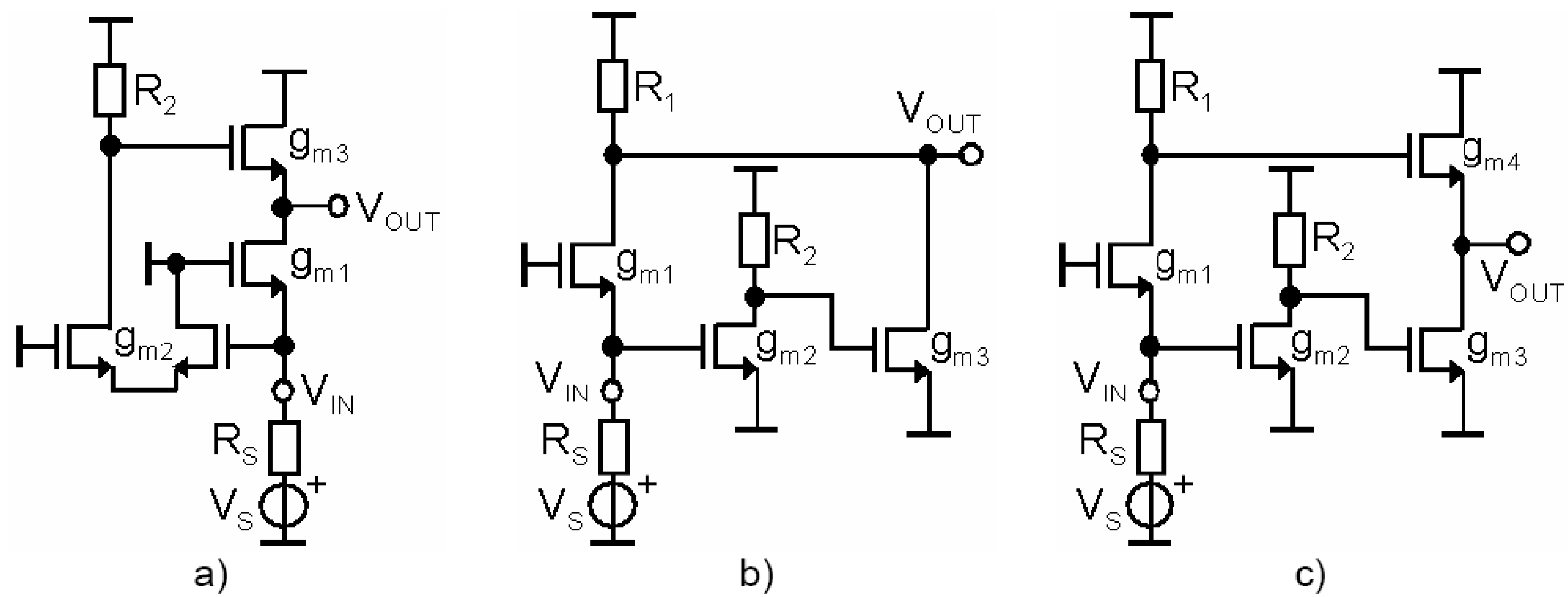
Chip photo



Measurement Results



Other possible topologies



[Bruccoleri et al., Springer, 2005]

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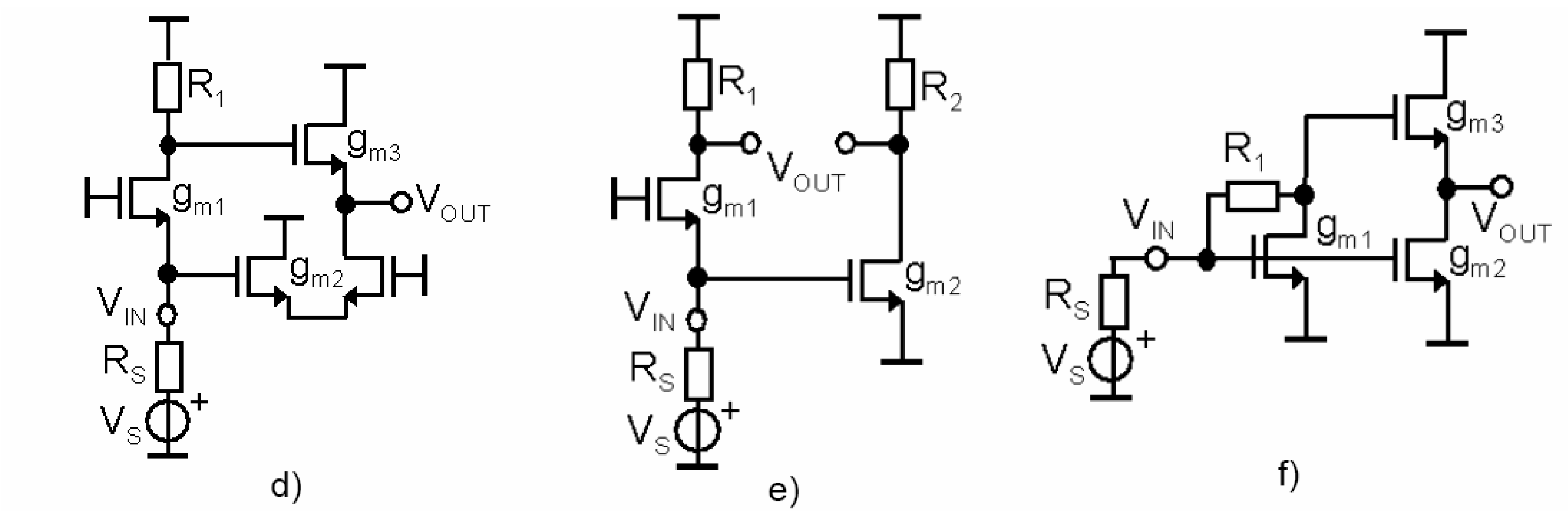

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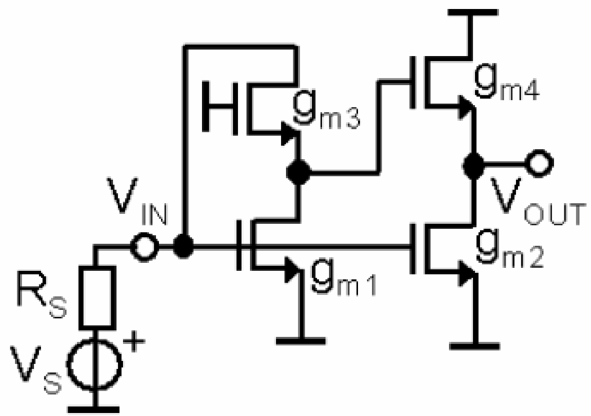
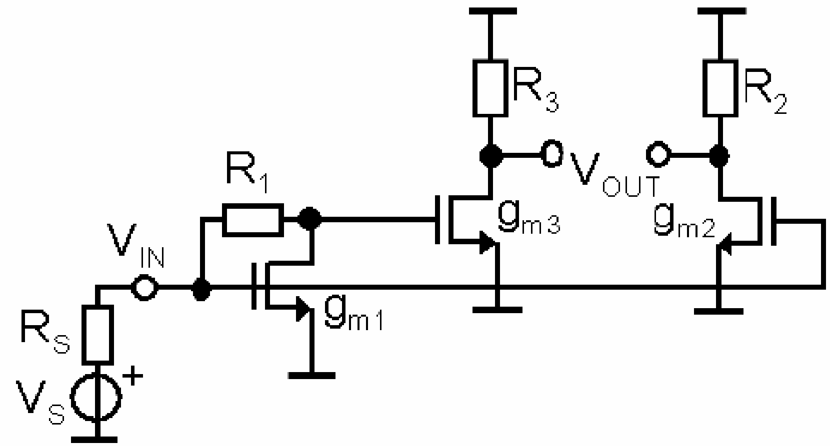
Other possible topologies





[Bruccoleri et al., Springer, 2005]

Summary: noise canceling

<u>Wideband Low-Noise Technique:</u>

- Matching-device noise cancels: NF & match *de*coupled!
- Wideband sub 3dB NF possible
- Good stability (feed-forward)
- Variable gain @ constant match possible

- Creates a degree of freedom,
- Does not violate the laws of nature
- Many possible topologies

references

- Bruccoleri, F., Klumperink, E.A.M., Nauta, B." Wide-Band CMOS Low-Noise Amplifier Exploiting Thermal-Noise Canceling" IEEE Journal of Solid-State Circuits, Vol. 39, No. 2, pp. 275 -282, February 2004.

- Bruccoleri, F., Klumperink, E.A.M., Nauta, B. "Wideband Low Noise Amplifiers exploiting thermal noise cancelling" Book, Kluwer/Springer 2005, ISBN 1-4020-3187-4

- Blaakmeer, S.C., Klumperink, E.A.M., Leenaerts, D.M.W., Nauta, B."A wideband Noise-Canceling CMOS LNA exploiting a transformer" Digest of papers of the 2006 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium,paper, June 2006, San Fransisco, CA.. USA

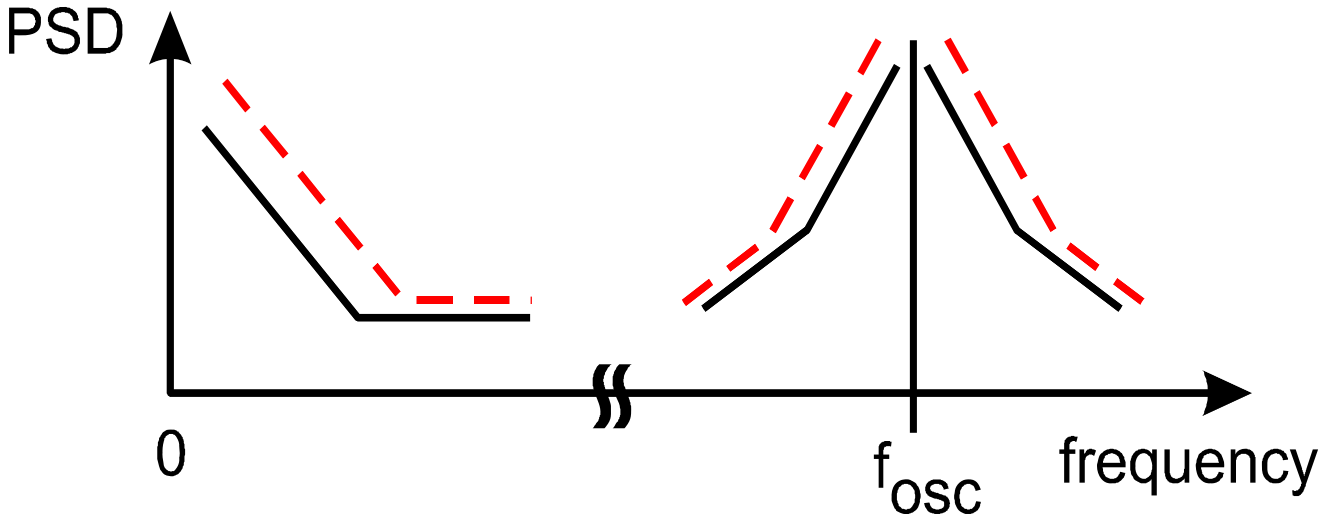
Outline

- Introduction
  - RF System trend
  - CMOS Technology trend
- Circuit Innovations
  - Noise canceling
  - **1/f noise reduction**
  - Distortion canceling
  - Switched Gm mixer

1/f noise

Is of increasing worry because:

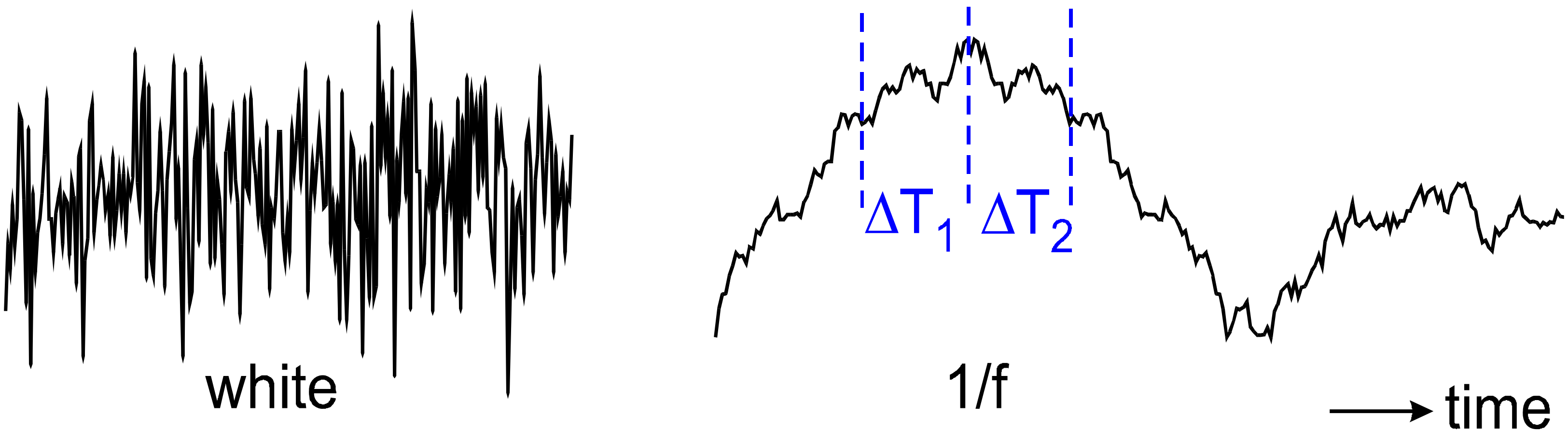
- smaller CMOS $\Rightarrow$ higher 1/f noise corner frequencies;
- 1/f noise can be up-converted to high frequencies (e.g. phase noise).



1/f noise

Reduce the *effect* of 1/f noise:

- amplifiers: chopping;
- switched capacitor: correlated double sampling;
- oscillators: symmetry of waveform *[Hajimiri]*



1/f noise

- Or reduce 1/f noise by area (large WxL)

- Burn power to preserve bandwidth

- 10dB less (1/f) noise = 10x more power dissipation

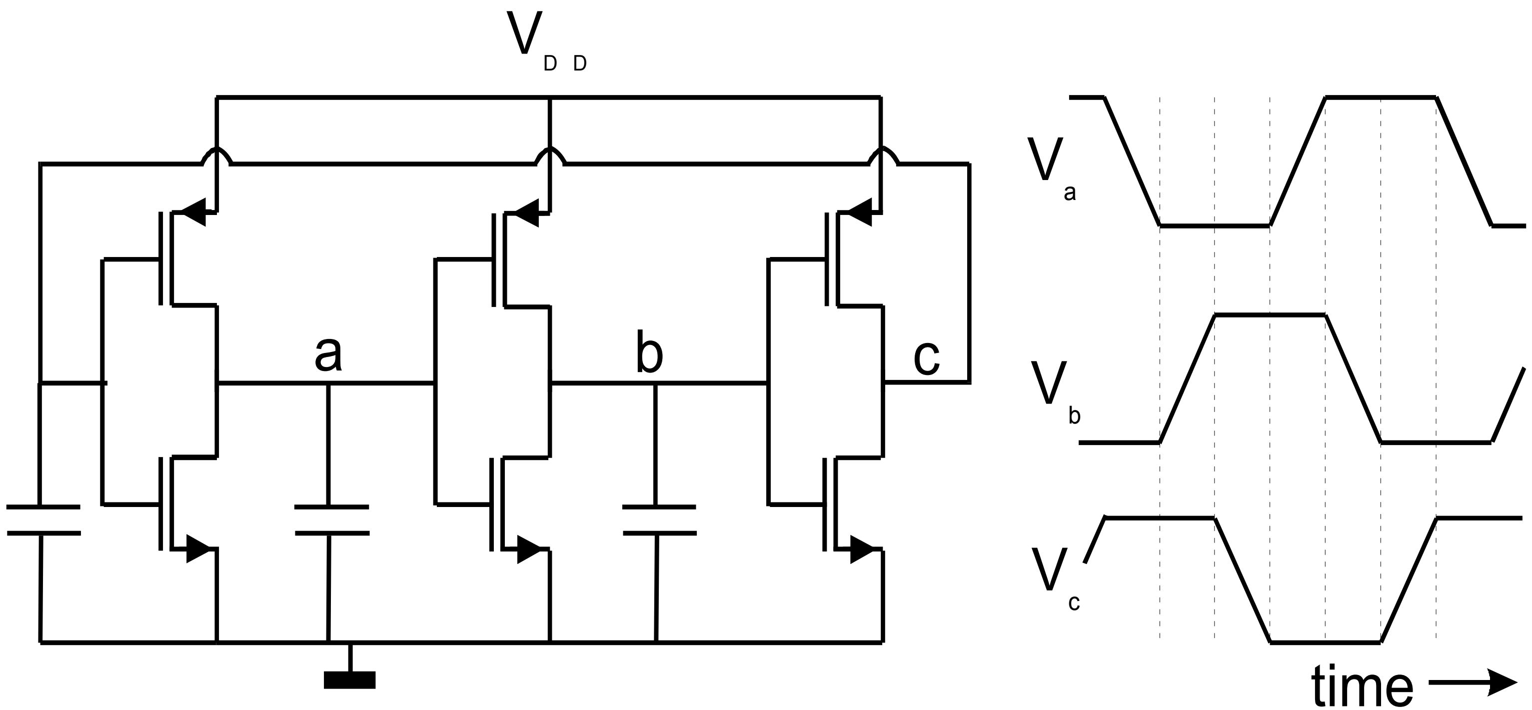
Or...

reduce the *correlation of 1/f noise itself* inside the MOSFETs

- lower 1/f noise
- lower dissipation!

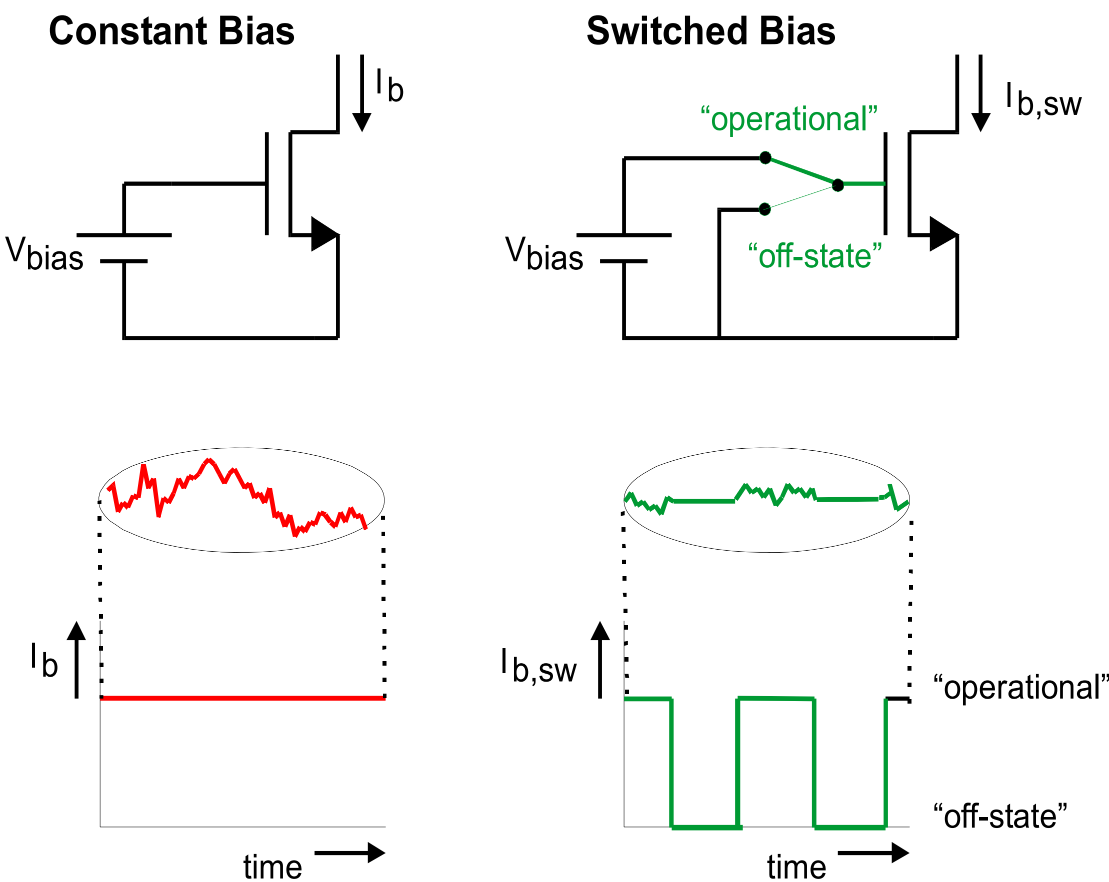
Effect found in the analysis of a CMOS ring oscillator:

Ring Oscillator

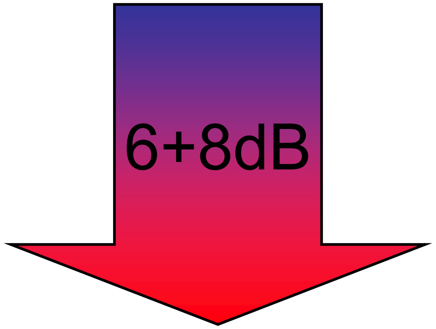


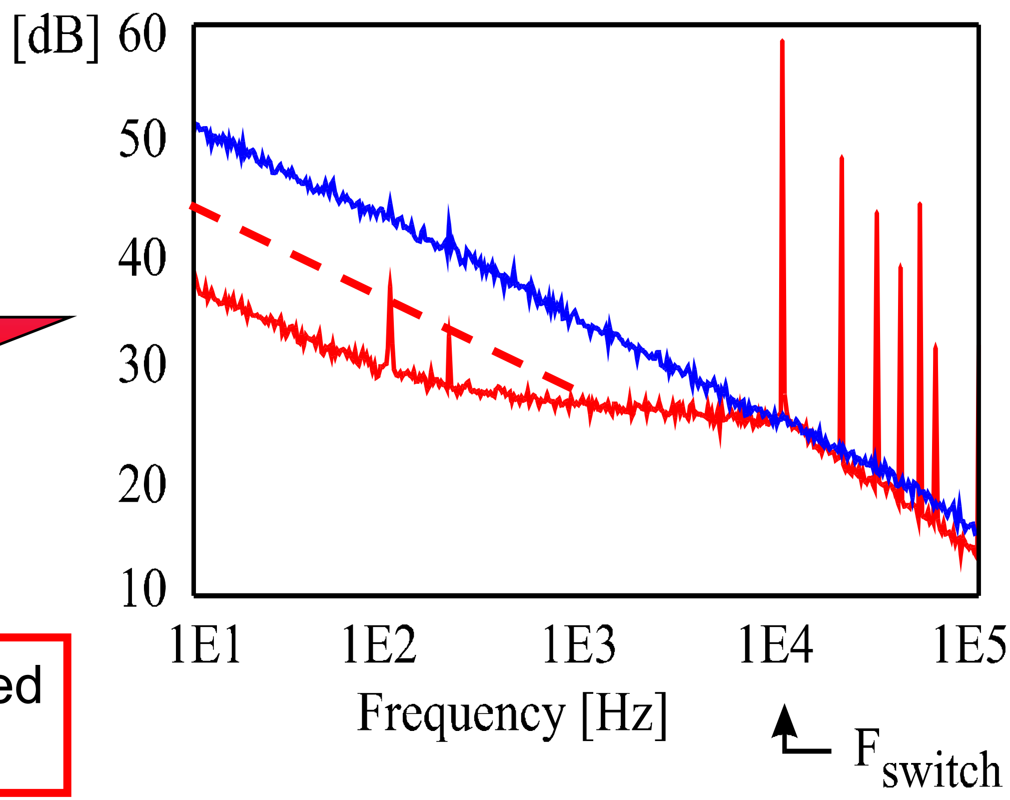
8 dB less close-in phase noise than
Expected / calculated / simulated

switching affects “1/f noise memory“ in transistors!



Intrinsic 1/f noise reduction



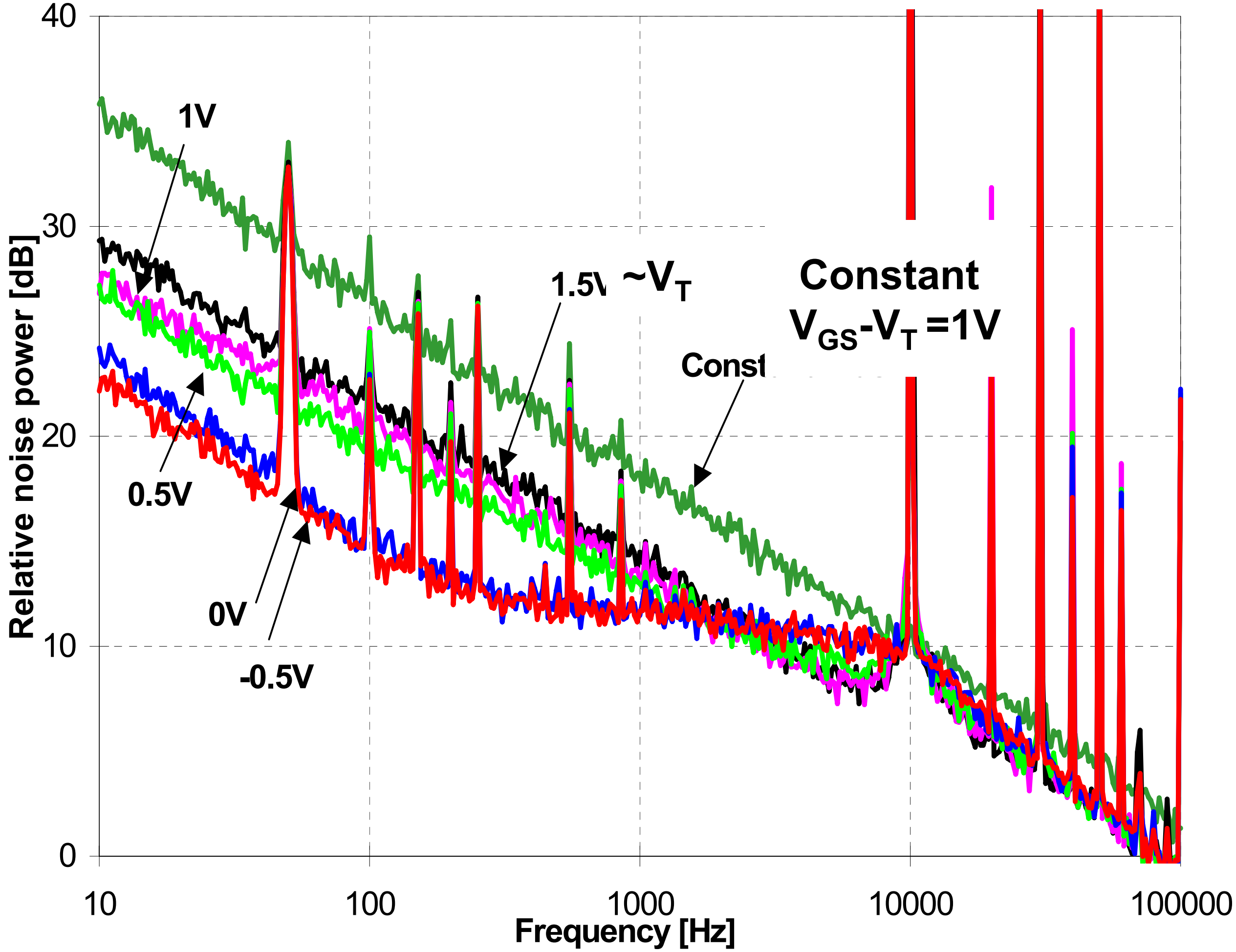


6dB=expected
8dB = extra!

Reduce 1/f noise **and** power dissipation

[see also : Bloom & Nemirovsky , Applied Physics Letters 1991]

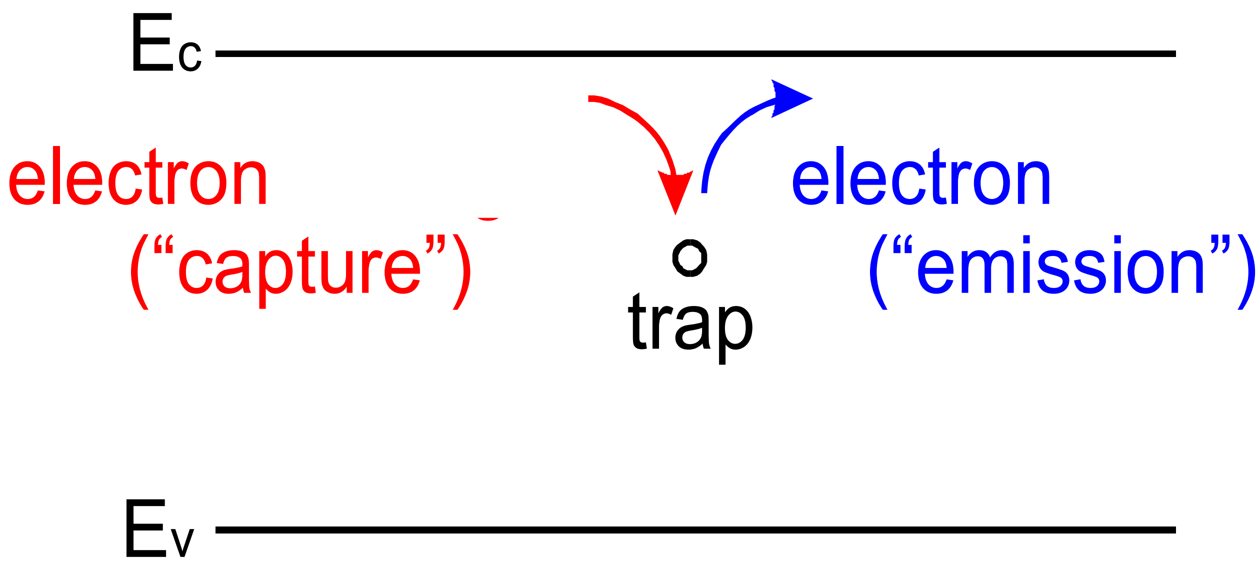
Change OFF-Voltage



Cycle to accumulation! (far below V_T)

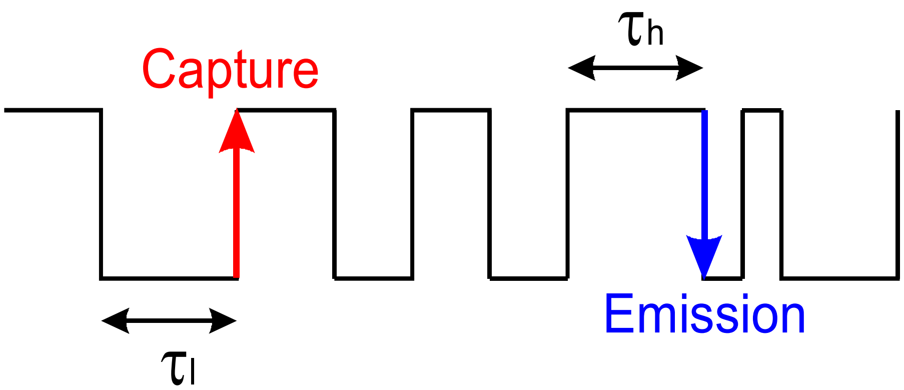
Modeling

McWhorter 1/f model. (1955)



Modeling

This yields a Random Telegraph Signal (RTS).

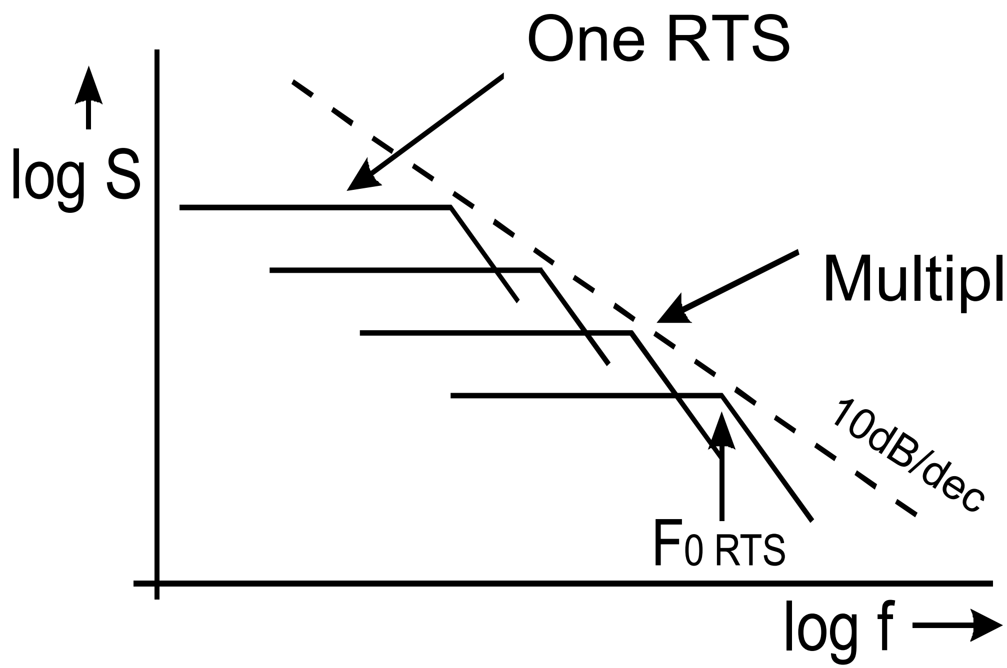


The probablity for a transition is:

$P_{lh}=1/\tau_l$ en $P_{hl}=1/\tau_h$

Modeling

How do you get a 1/f spectrum from multiple RTS?



Modeling - conclusions

- Oxide trapping -> RTS -> τ_c and τ_e
- τ_c and τ_e are bias dependent
- Changing dynamically τ_c and τ_e, explains observations
- Small devices: large spread due to few traps
- Small devices: The worse is improved, the best is getting a bit worse
- Large device: average of small devices (-8dB)

Summary: reduction of 1/f noise

- Effect previously unknown to designers
- Typical improvement: -8dB
- Deeper off switching helps
- Found in all technologies 10μm -> 0.12μm,
- Nmos and pmos,
- Small transistors -> spread
- More noise -> more reduction: up to 20dB
- Works at least up to 3 GHz
- Bias dependent statistical model gives realistic results

- It’s not in your simulator!

References

- Basic discovery:

  I. Bloom and Y. Nemirovsky, “1=f noise reduction of metal-oxidesemiconductor transistors by cycling from inversion to accumulation,” Applied Physics Letters, vol. 58, no. 15, pp. 1664–1666, Apr. 1991.

- Overview article for circuit designers:

  A.P. van der Wel , E.A.M. Klumperink , J. Kolhatkar , E. Hoekstra, M. Snoeij , C. Salm, H. Wallinga and B. Nauta “Low Frequency Noise Phenomena in Switched MOSFETs”, IEEE Journal of Solid State Circuits, Vol. 42, No.3, March 2007.

Outline

- Introduction
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- Circuit Innovations
  - Noise canceling
  - 1/f noise reduction
  - **Distortion canceling**
  - Switched Gm mixer

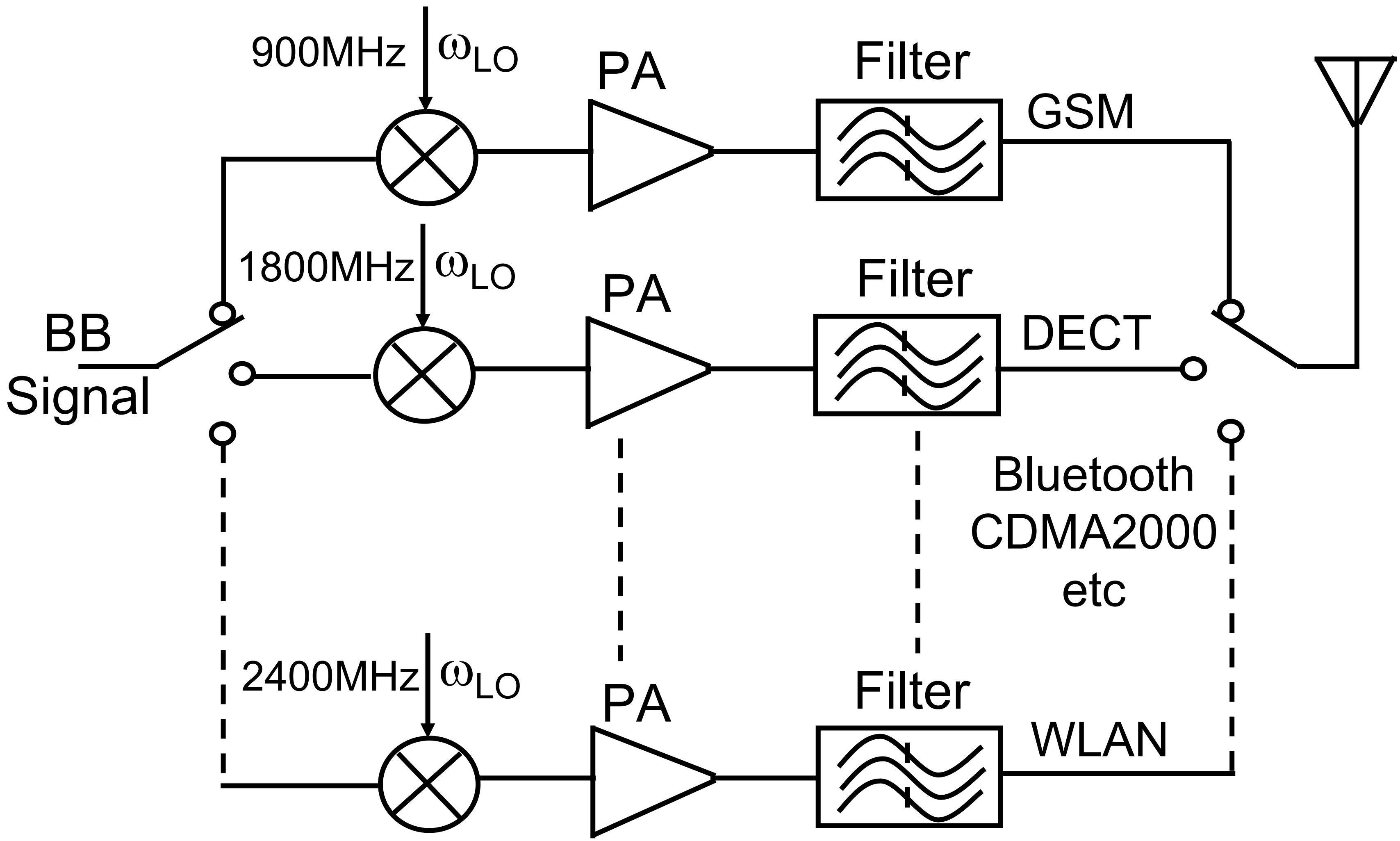
Distortion canceling technique

- Basic idea:
  - In differential circuits even harmonics are cancelled
  - Can we cancel more harmonics in an N path circuit?

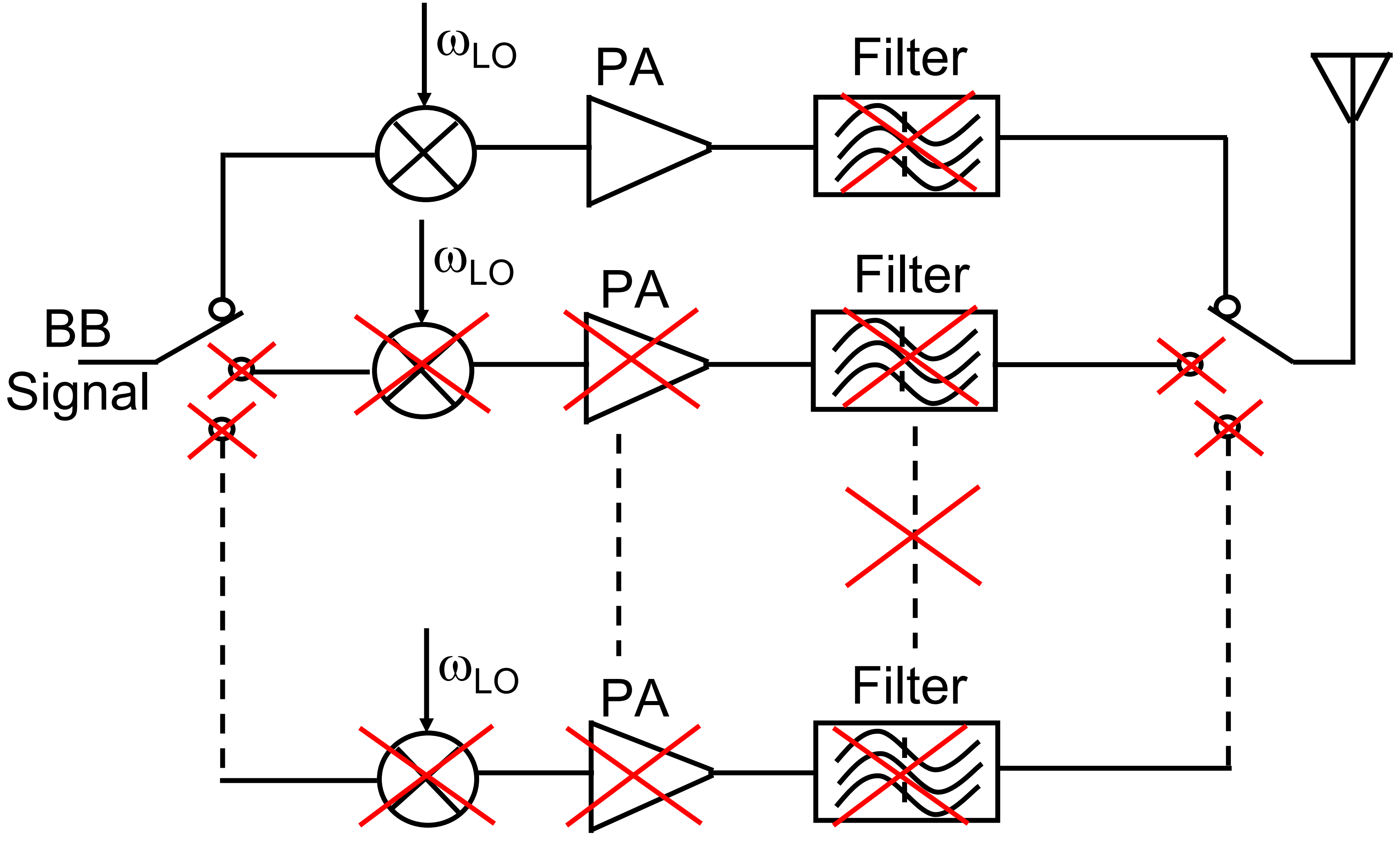
- For upconvertes
  - Using mulitiple paths
  - For wide band circuits & Software defined transmitters

- Alternative for filtering

Multi-standard Transmitter Architecture

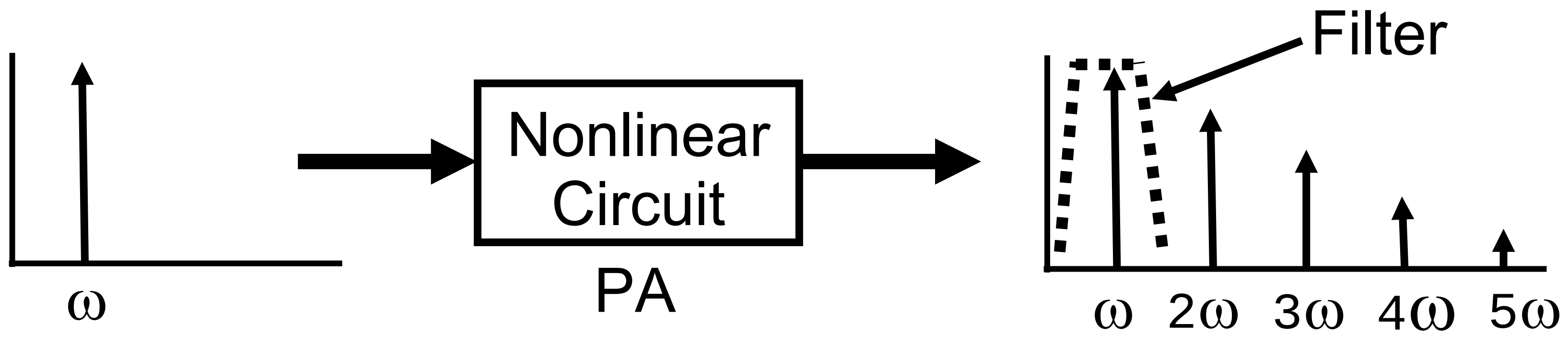


Multi-standard Transmitter Architecture



Why do we need a *filter?*

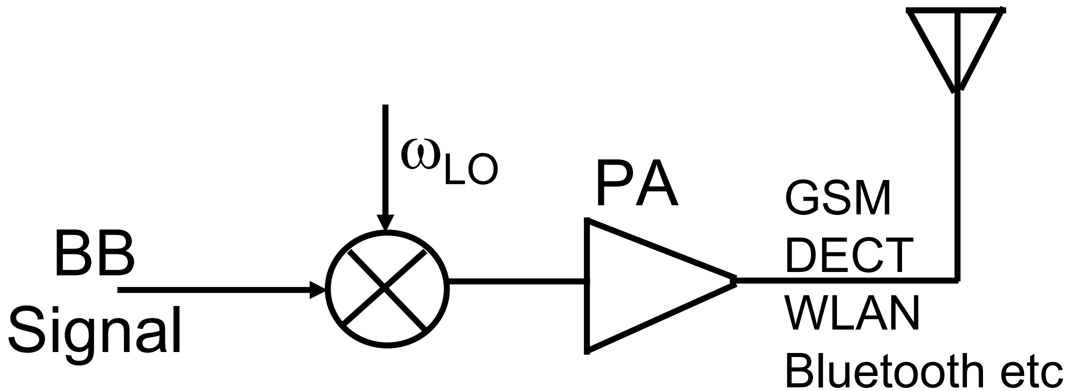
To remove unwanted harmonics



Dedicated filter for each standard

Dream:

One Flexible Upconverter, No Filters

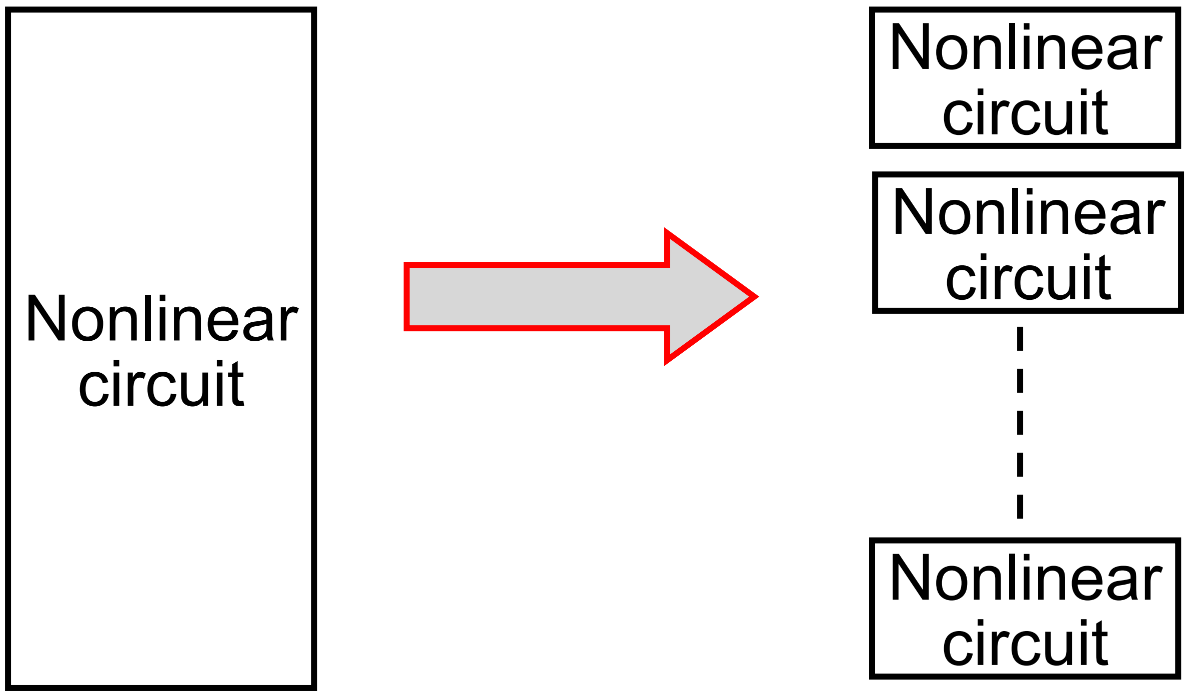


<u>How?</u>

"Polyphase Multipath Technique"

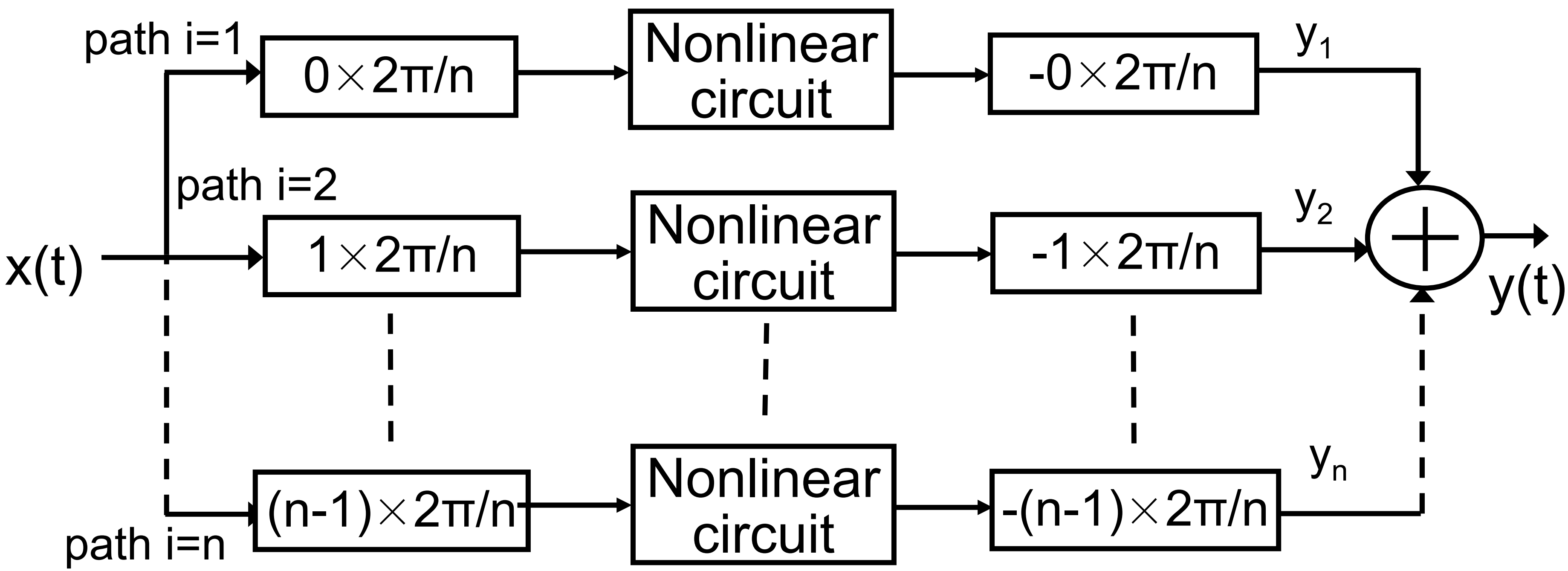
Theory of Polyphase Multipath (1)

Divide the nonlinear circuit into ‘n’ equal smaller pieces



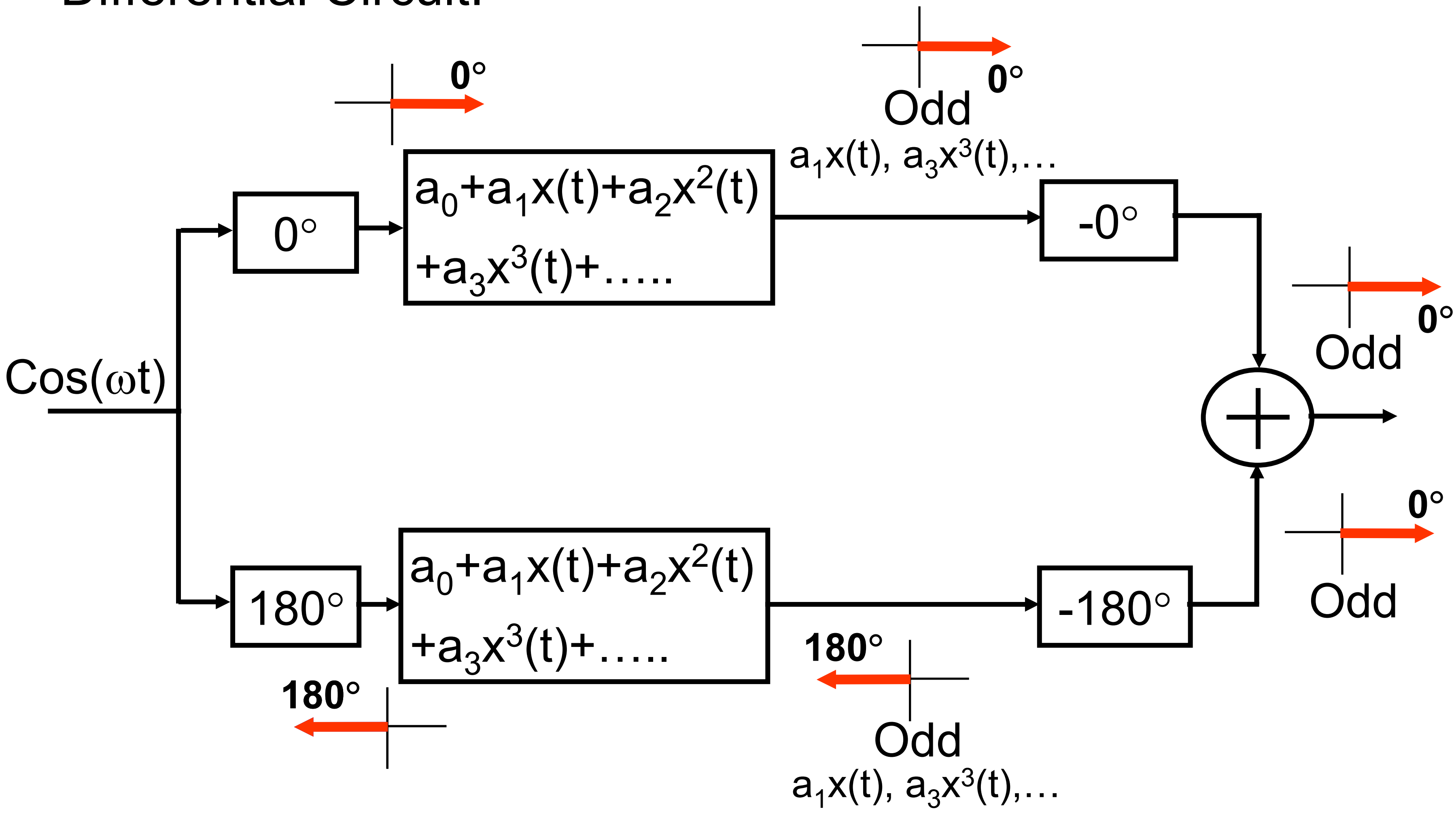
Theory of Polyphase Multipath (2)

Add equal but *opposite* phase shift before and after



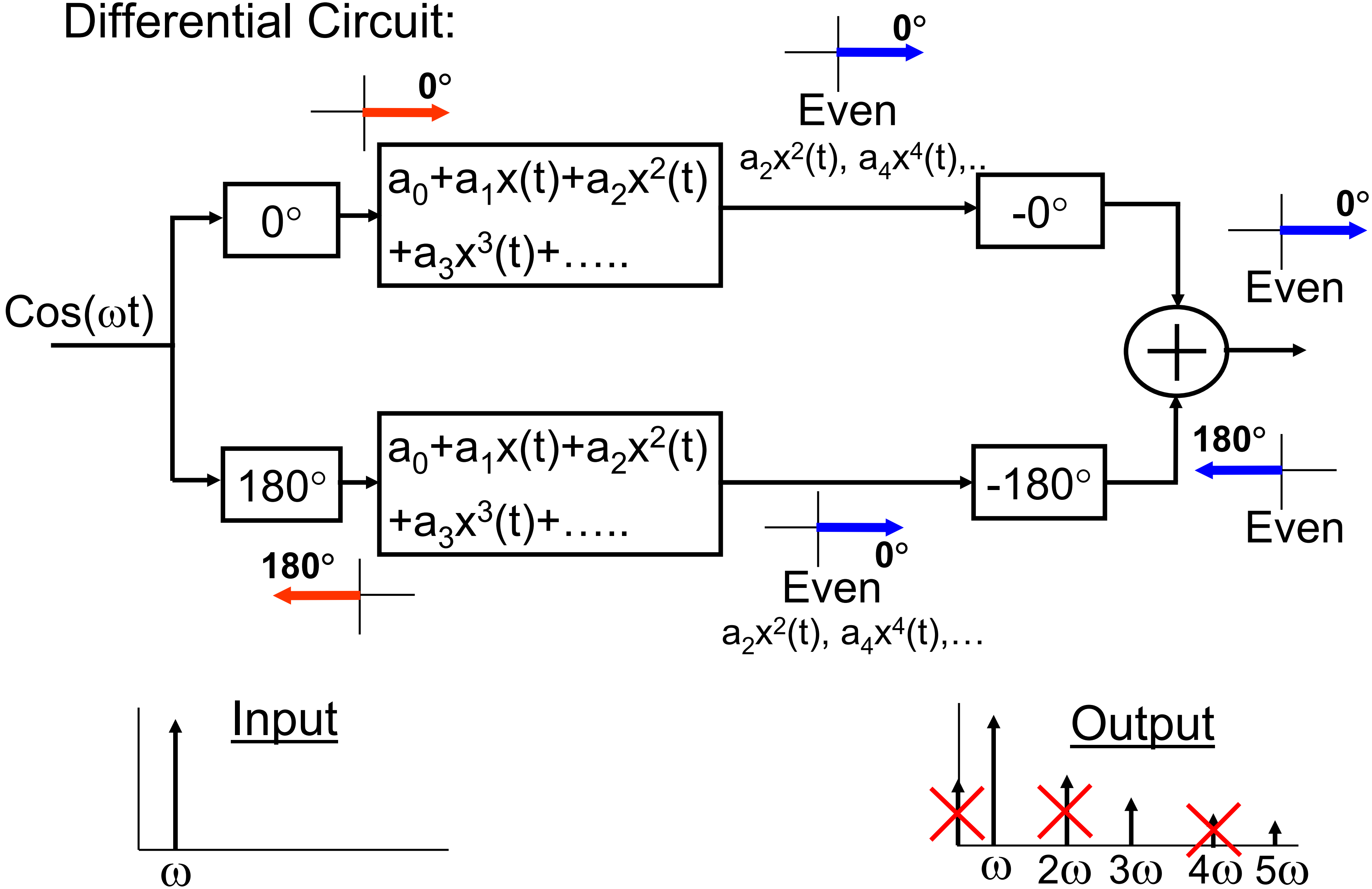
Polyphase 2-Path Circuit (1)

Differential Circuit:

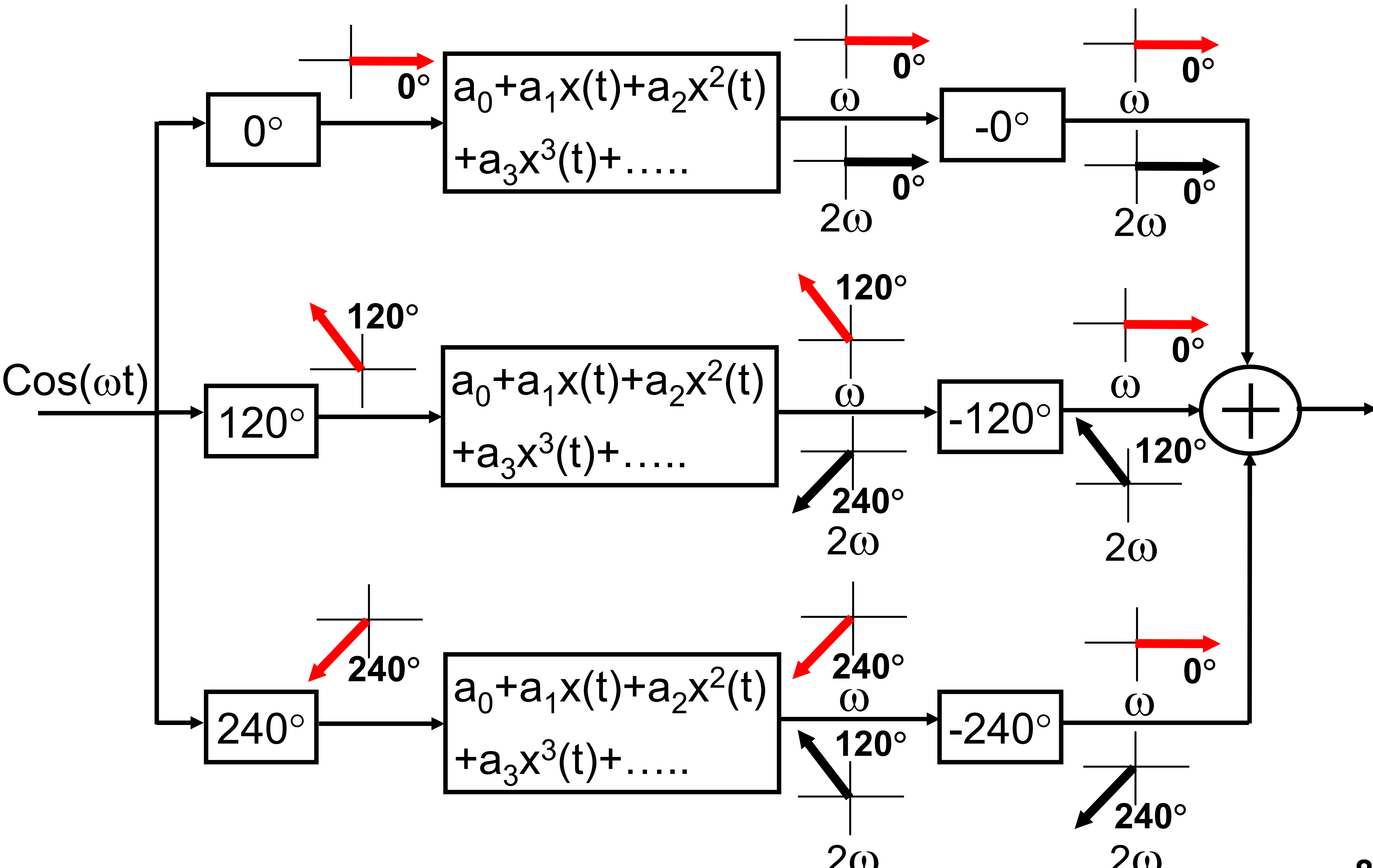


Polyphase 2-Path Circuit (2)

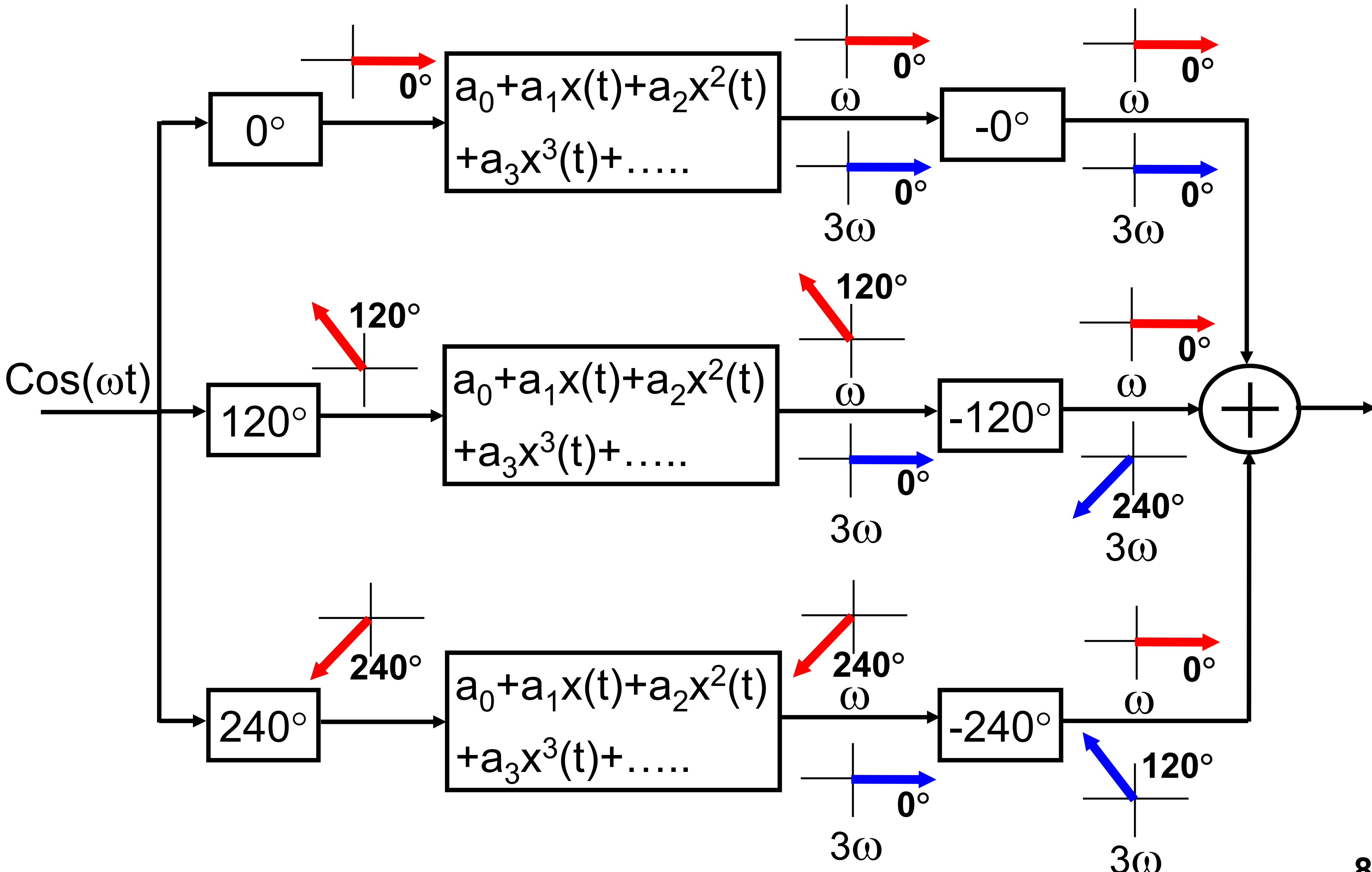
Differential Circuit:



Polyphase 3-Path Circuit (1)

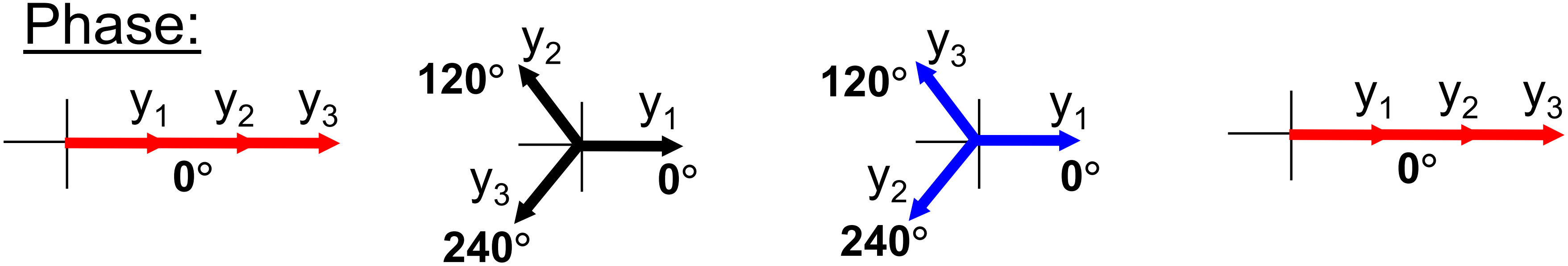


Polyphase 3-Path Circuit (2)



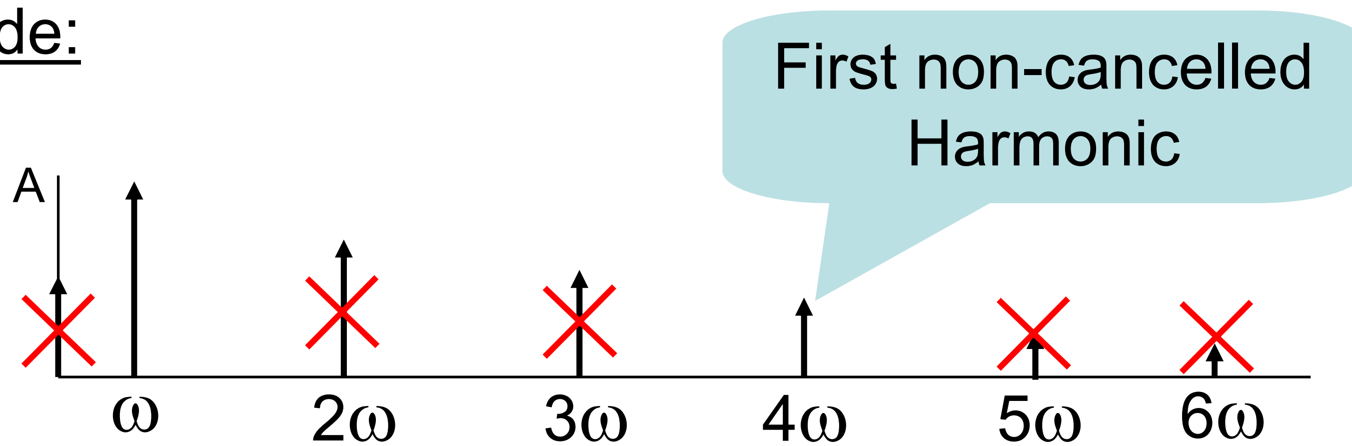
Output: Polyphase 3-Path

Phase:

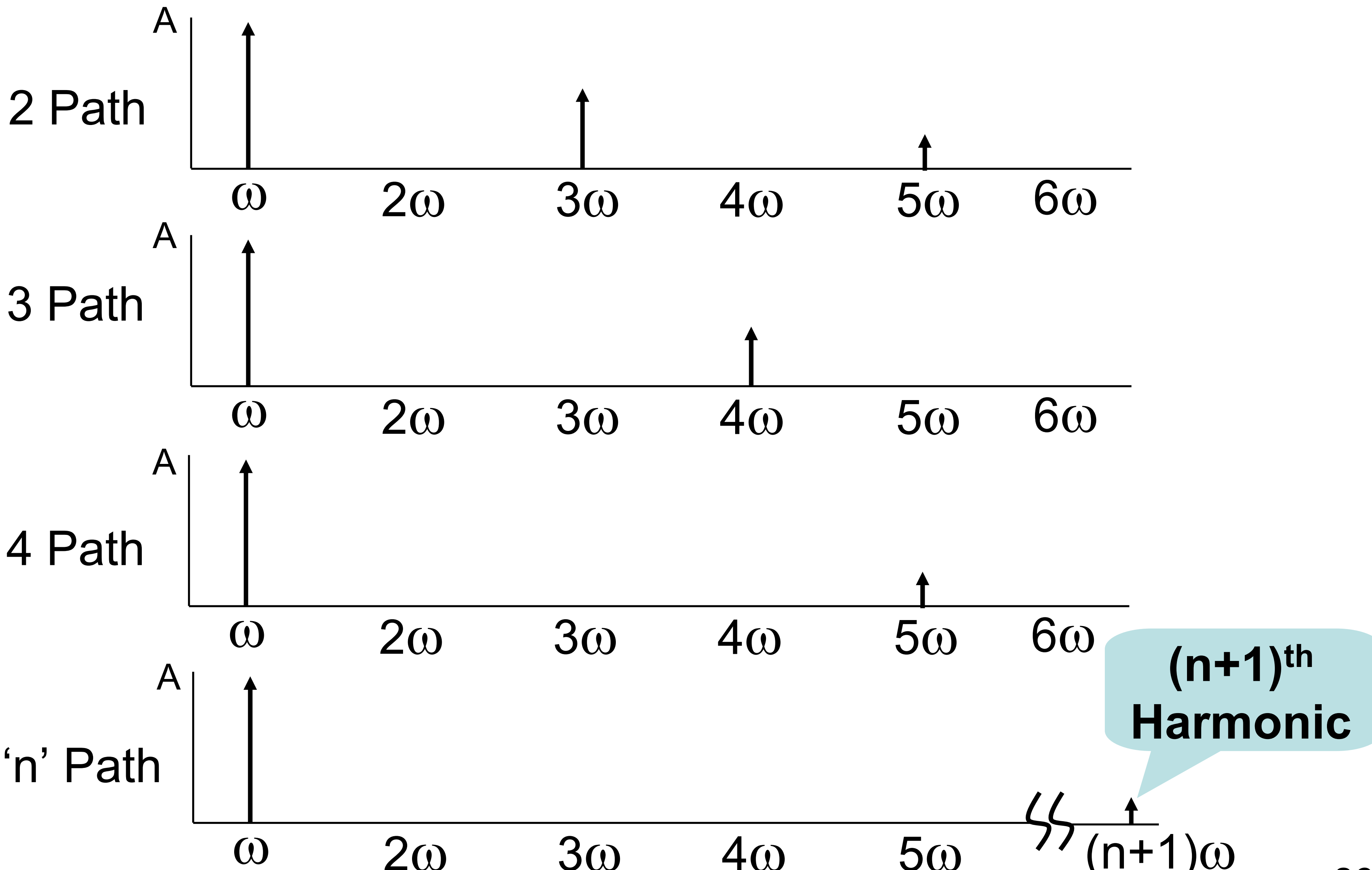


Fundamental **2nd Harmonic** **3rd Harmonic** **4th Harmonic**

Magnitude:

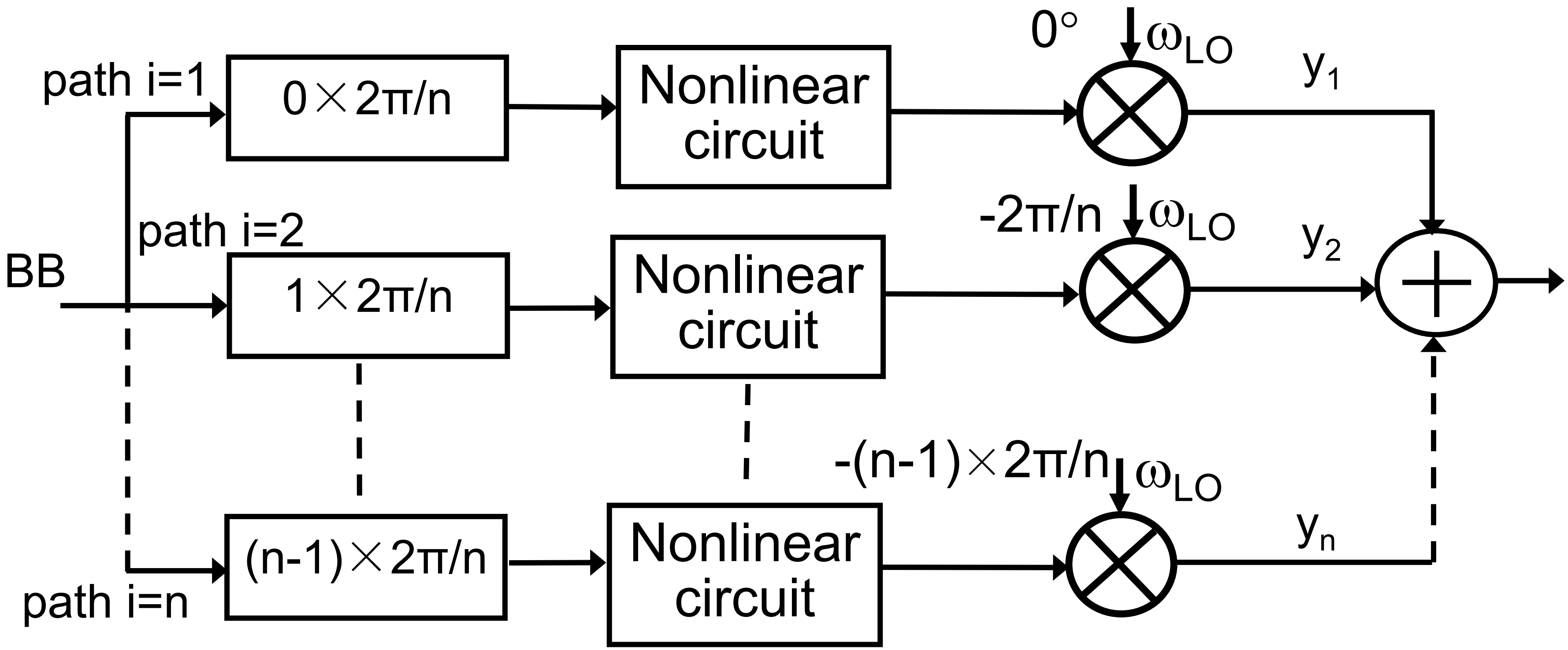


And now increase the number of paths…



Problem: Bandwidth of Phase Shifter

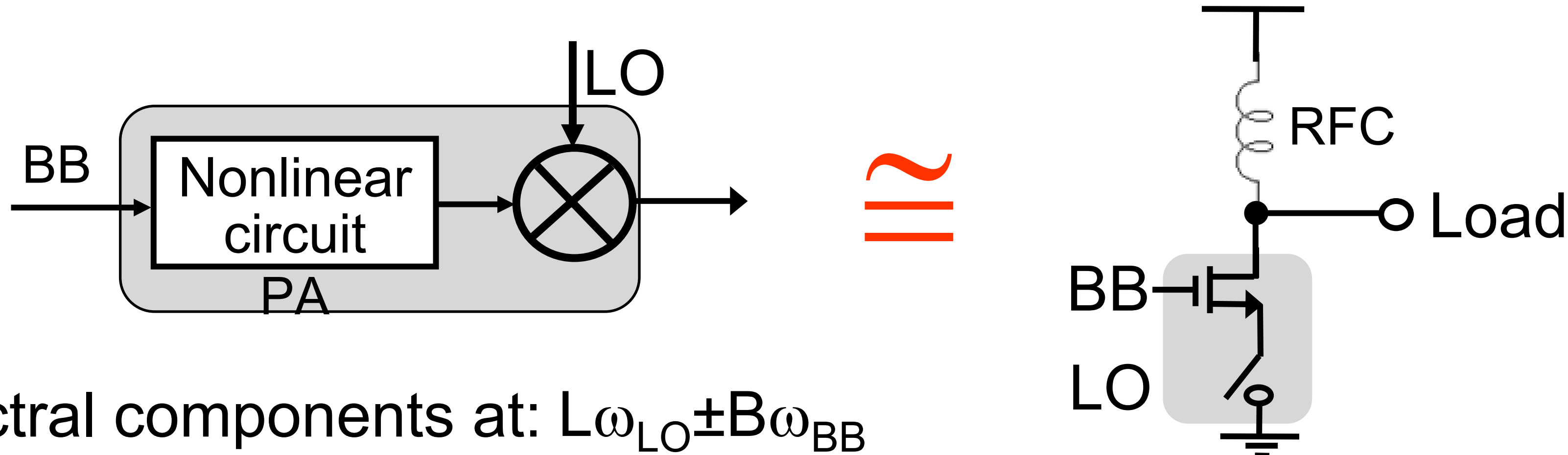
<u>Solution</u>: Mixer (transparent for LO Phase)



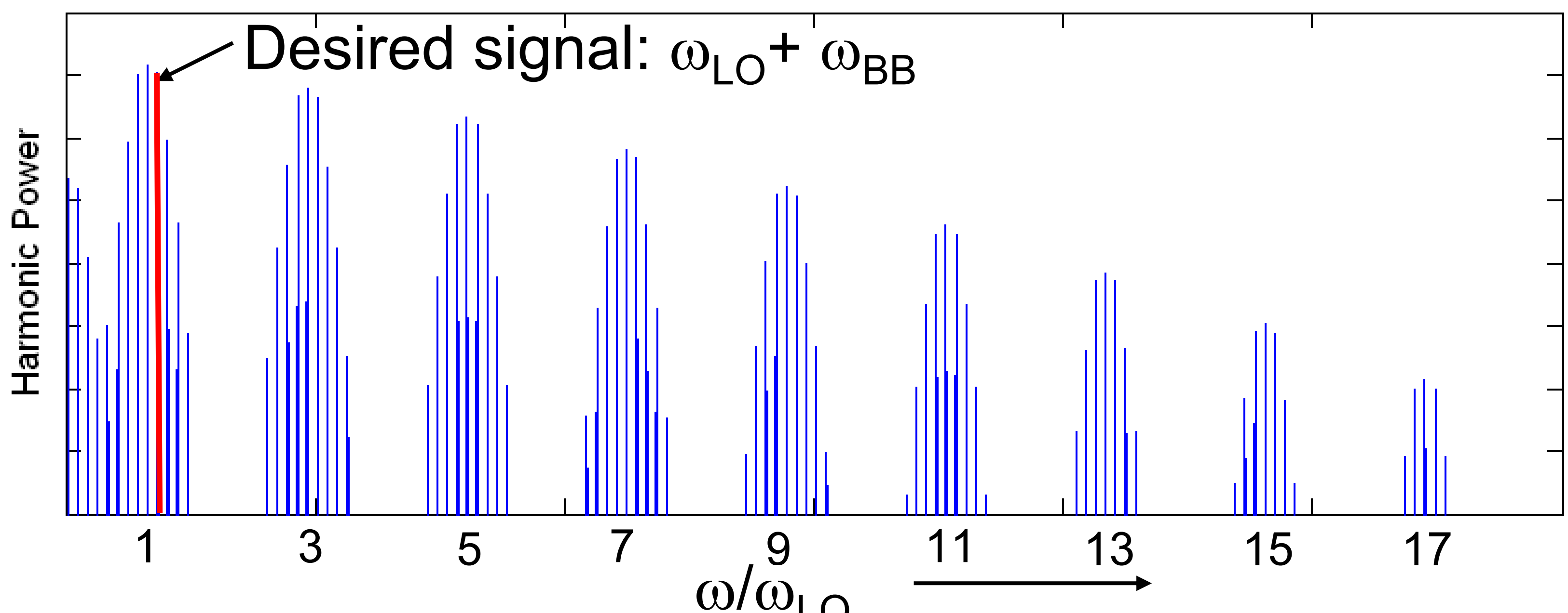
Wideband band phase shift but also upconversion

Basic Power Upconverter

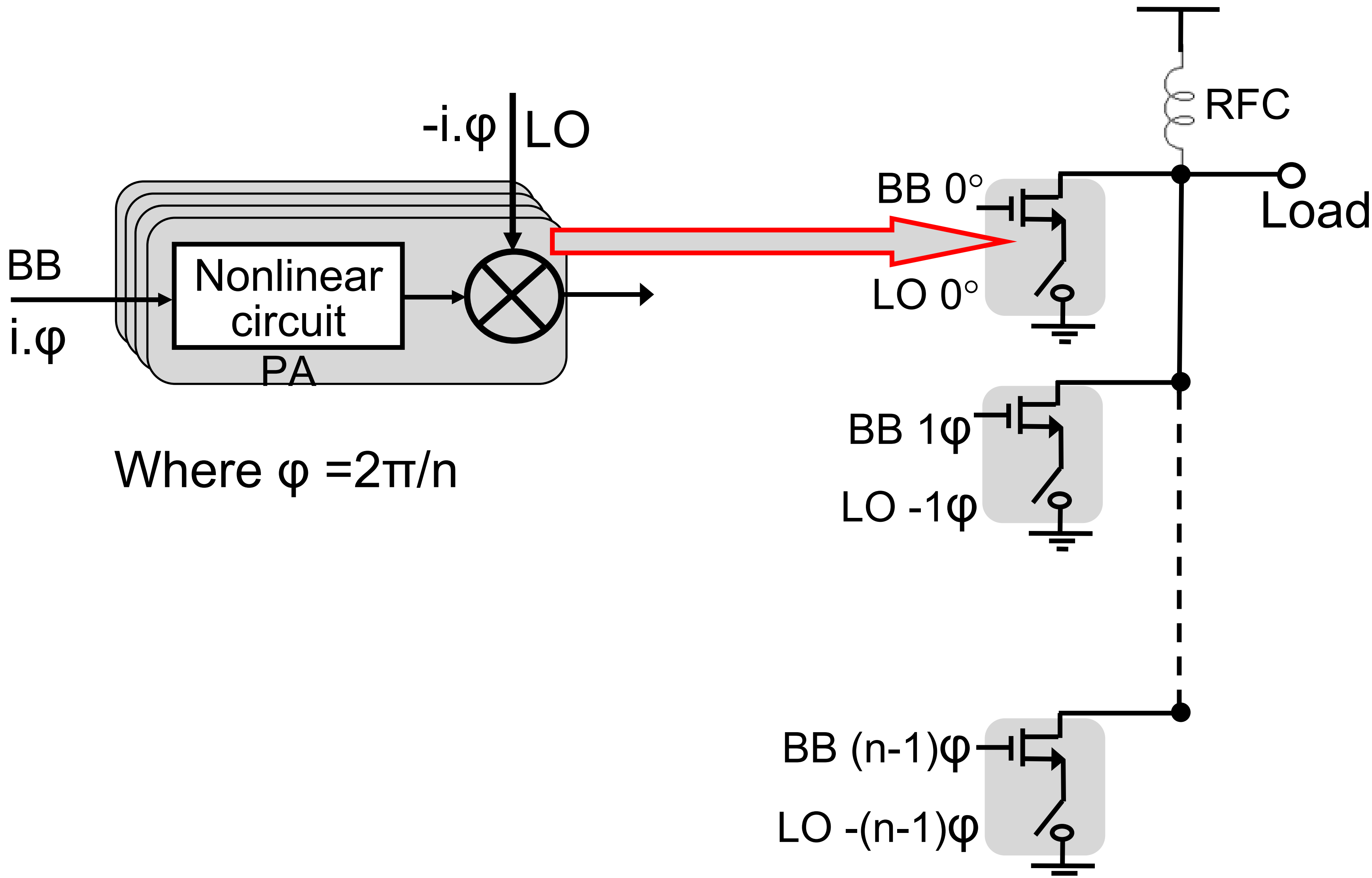
Combined functionalities of Power Amplifier and mixer



Spectral components at: $L\omega_{LO} \pm B\omega_{BB}$

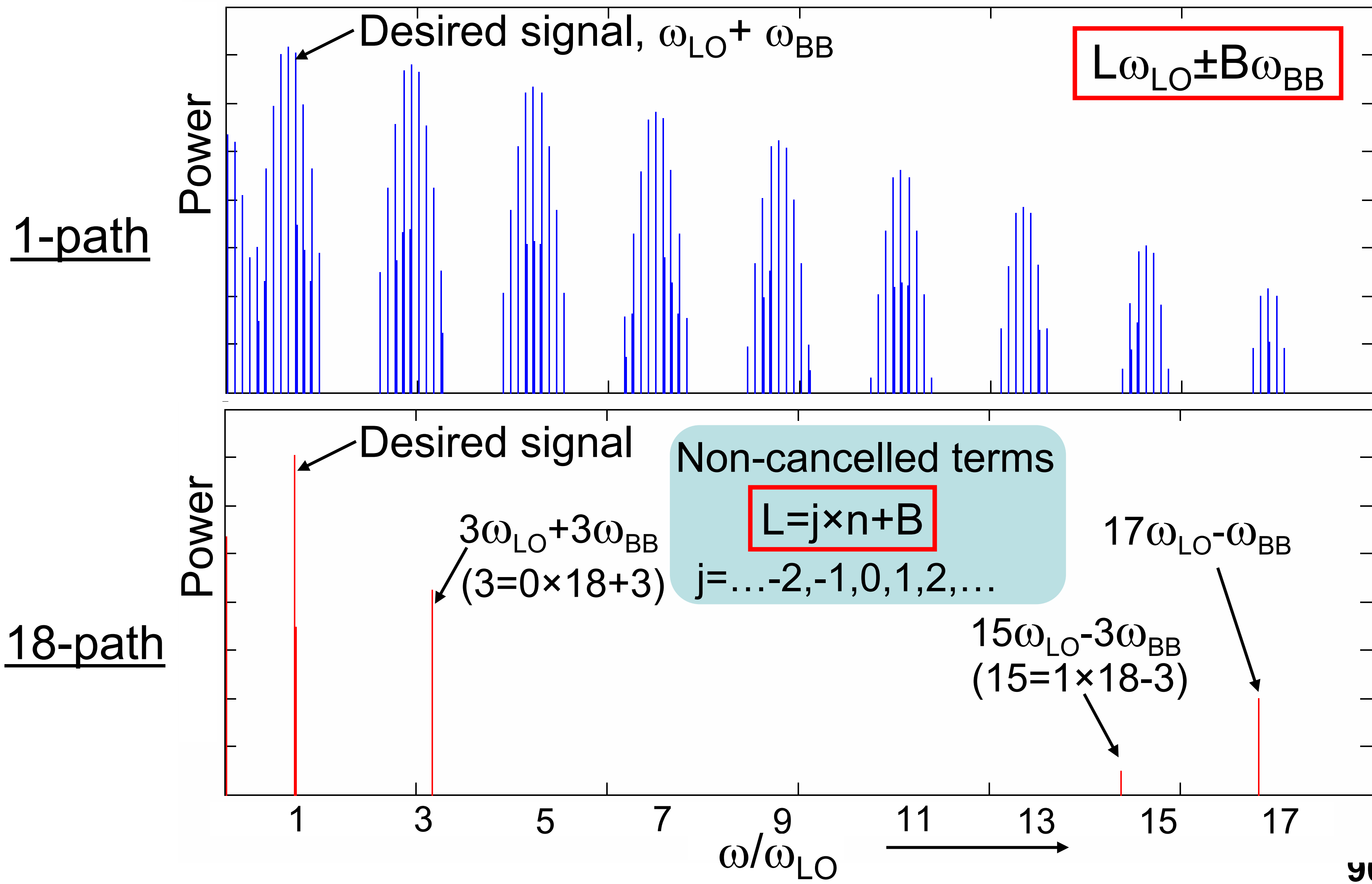


n-Path Power Upconverter



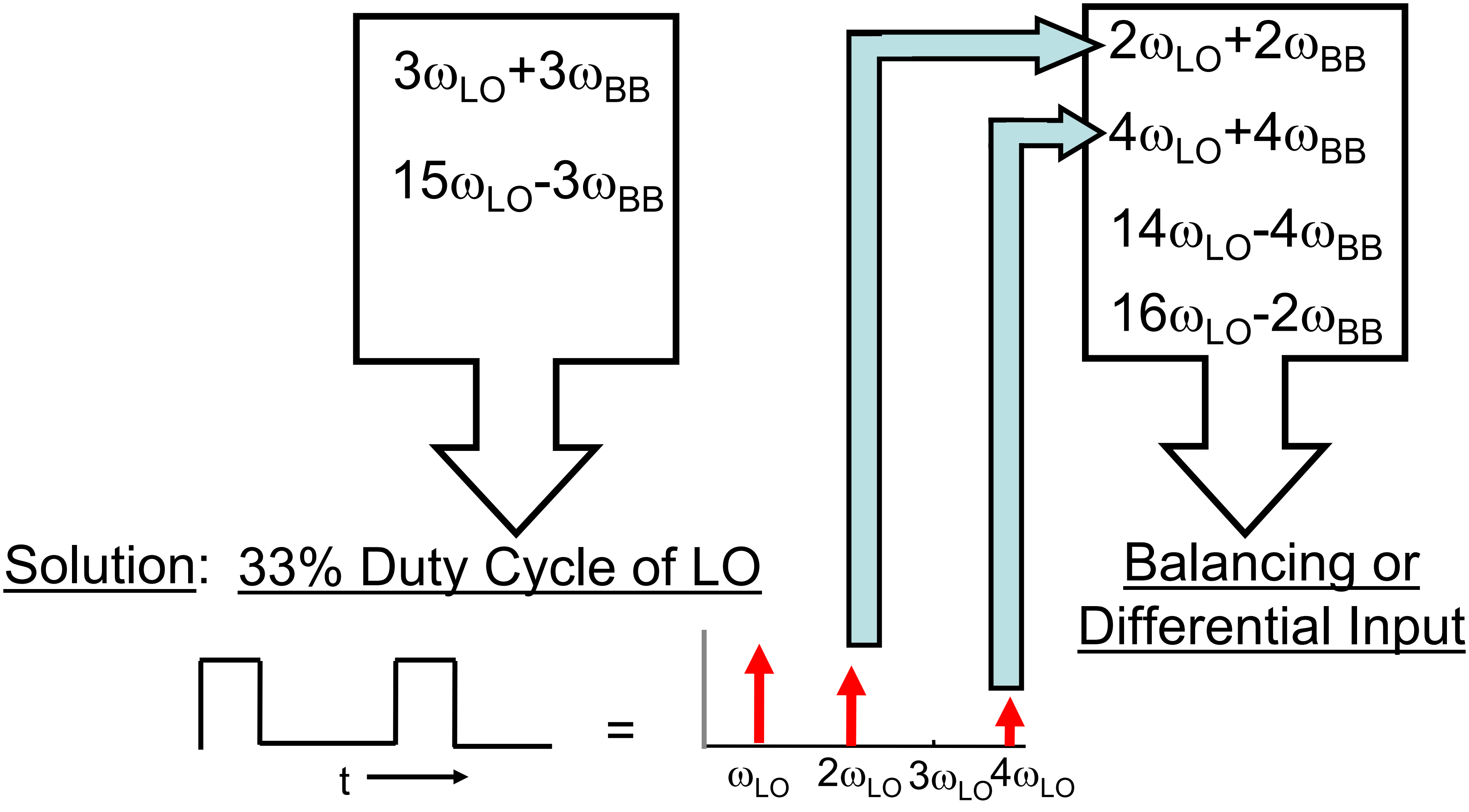
Where $\varphi = 2\pi/n$

Cancellation of Harmonics and Sidebands

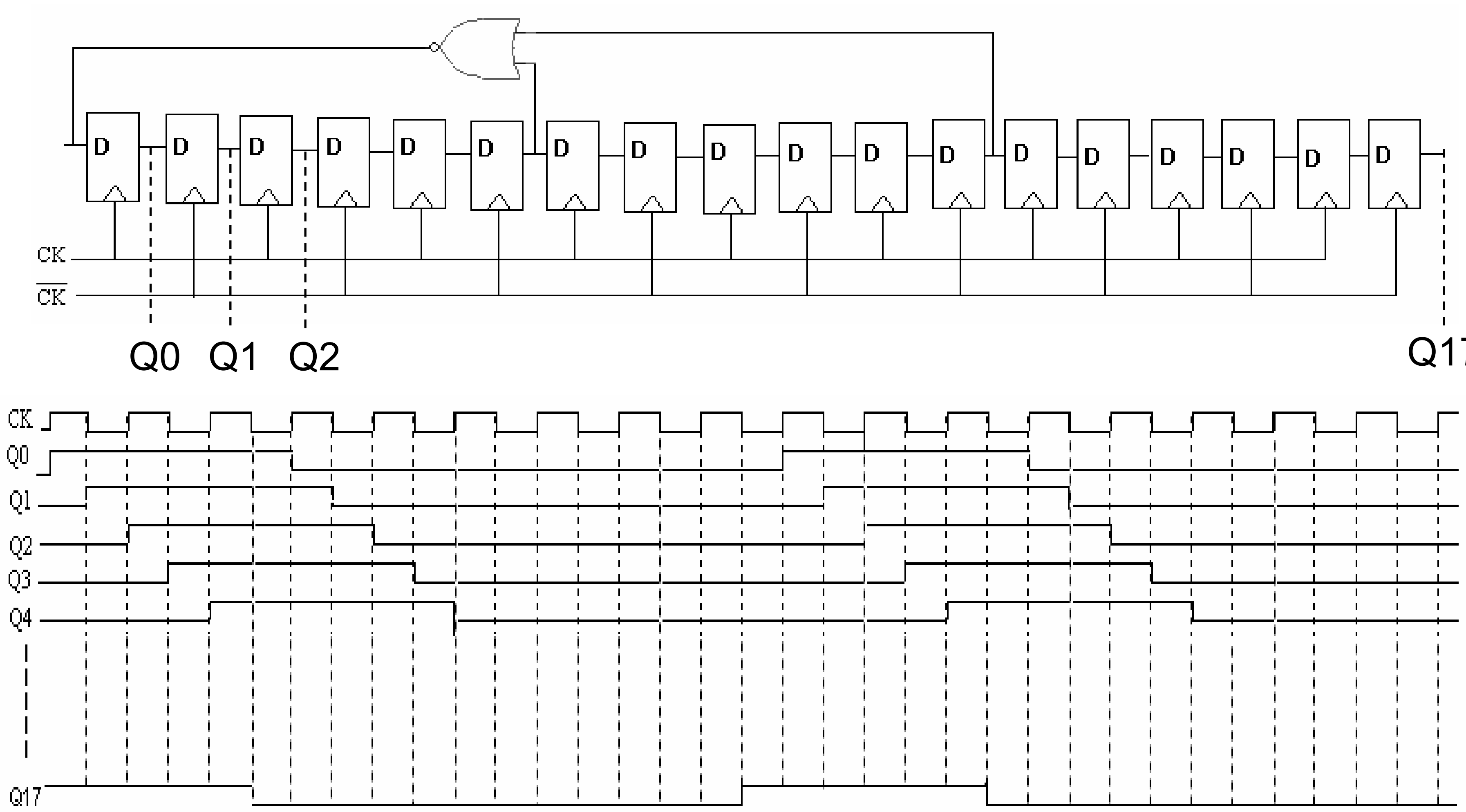


Solution: 1/3 Duty Cycle of LO

Problem: Uncancelled products

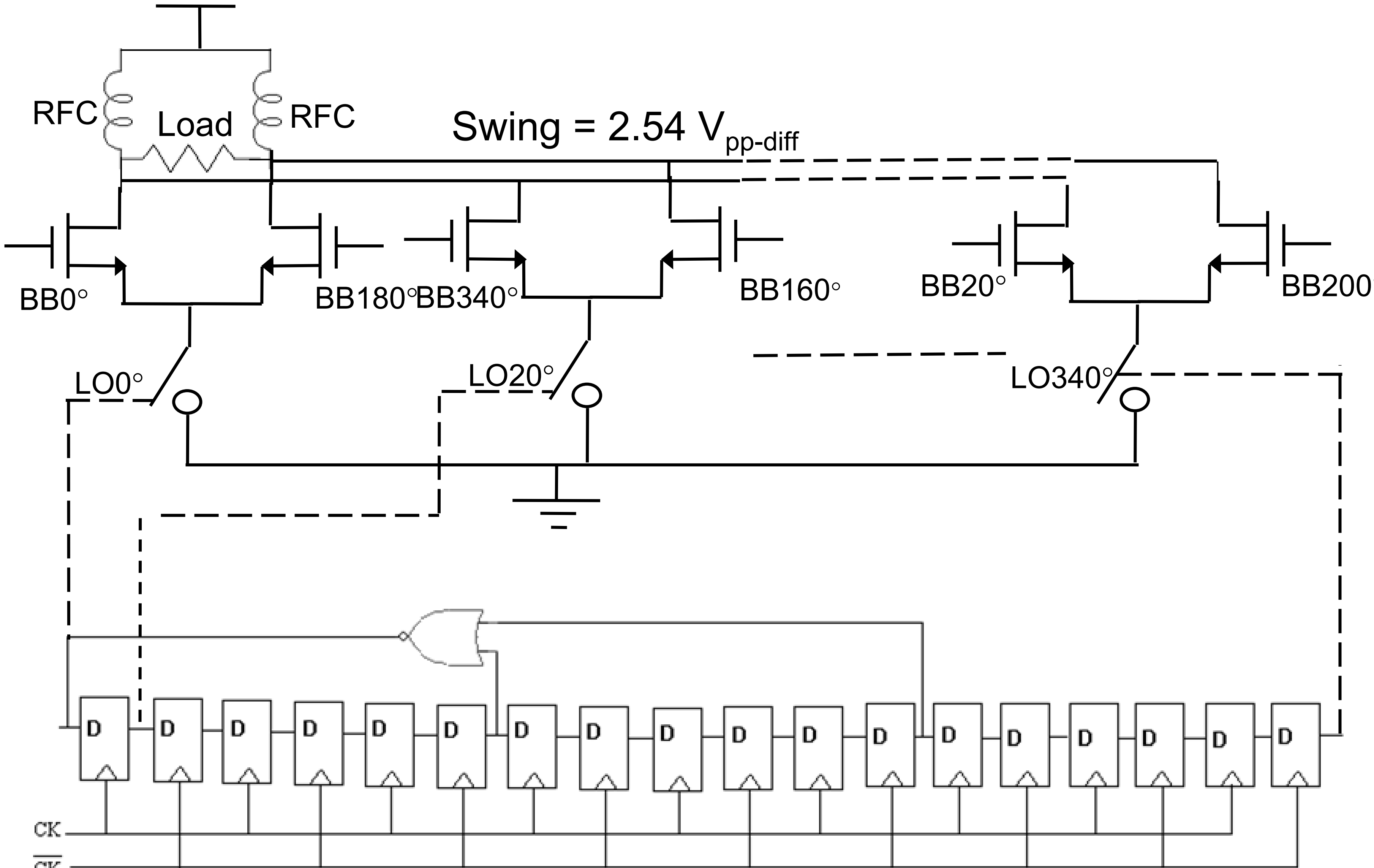


LO Phase Generation on Testchip

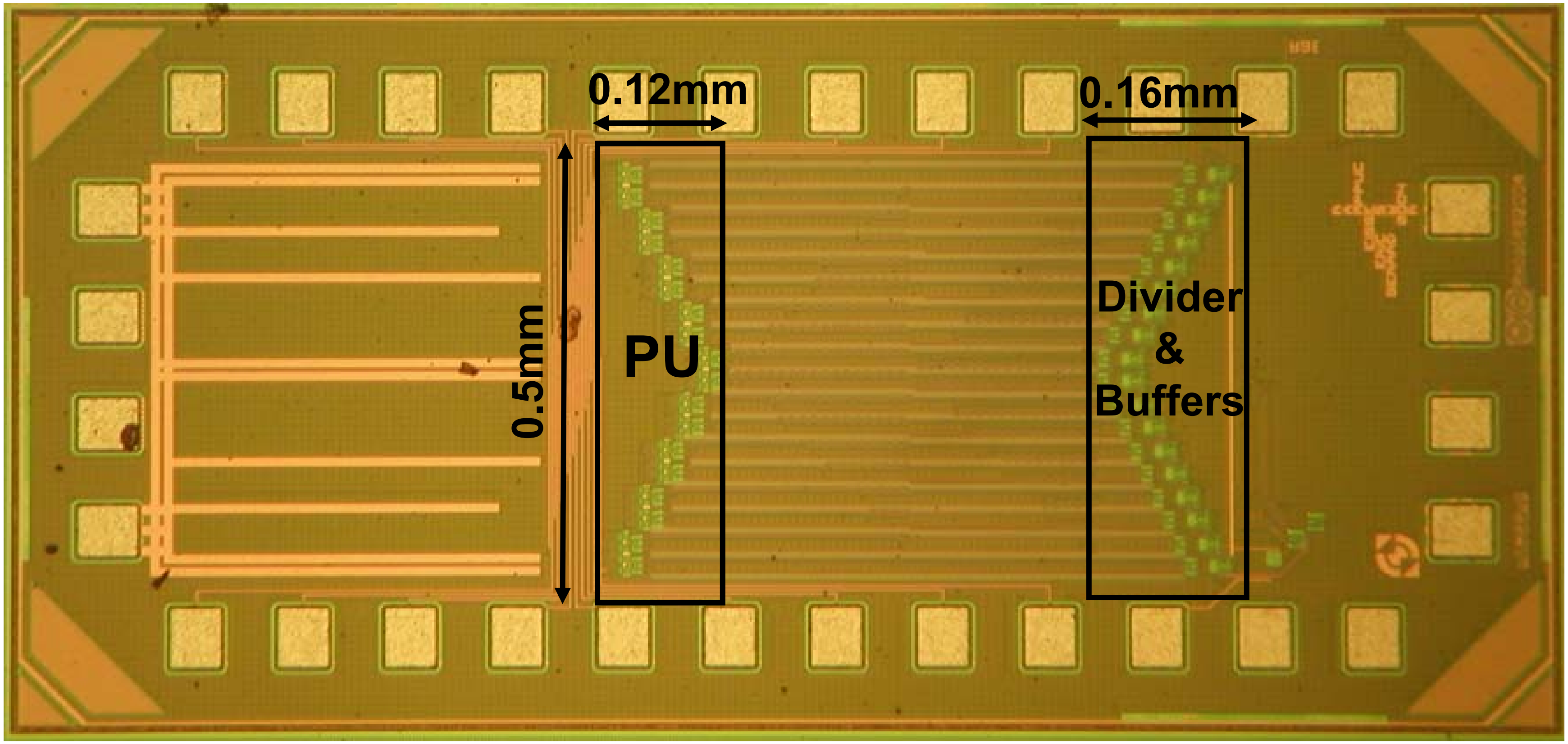


Clock CK at 9x LO ("brute force")

Power Upconverter: 18 paths



Demonstrator Chip Micrograph

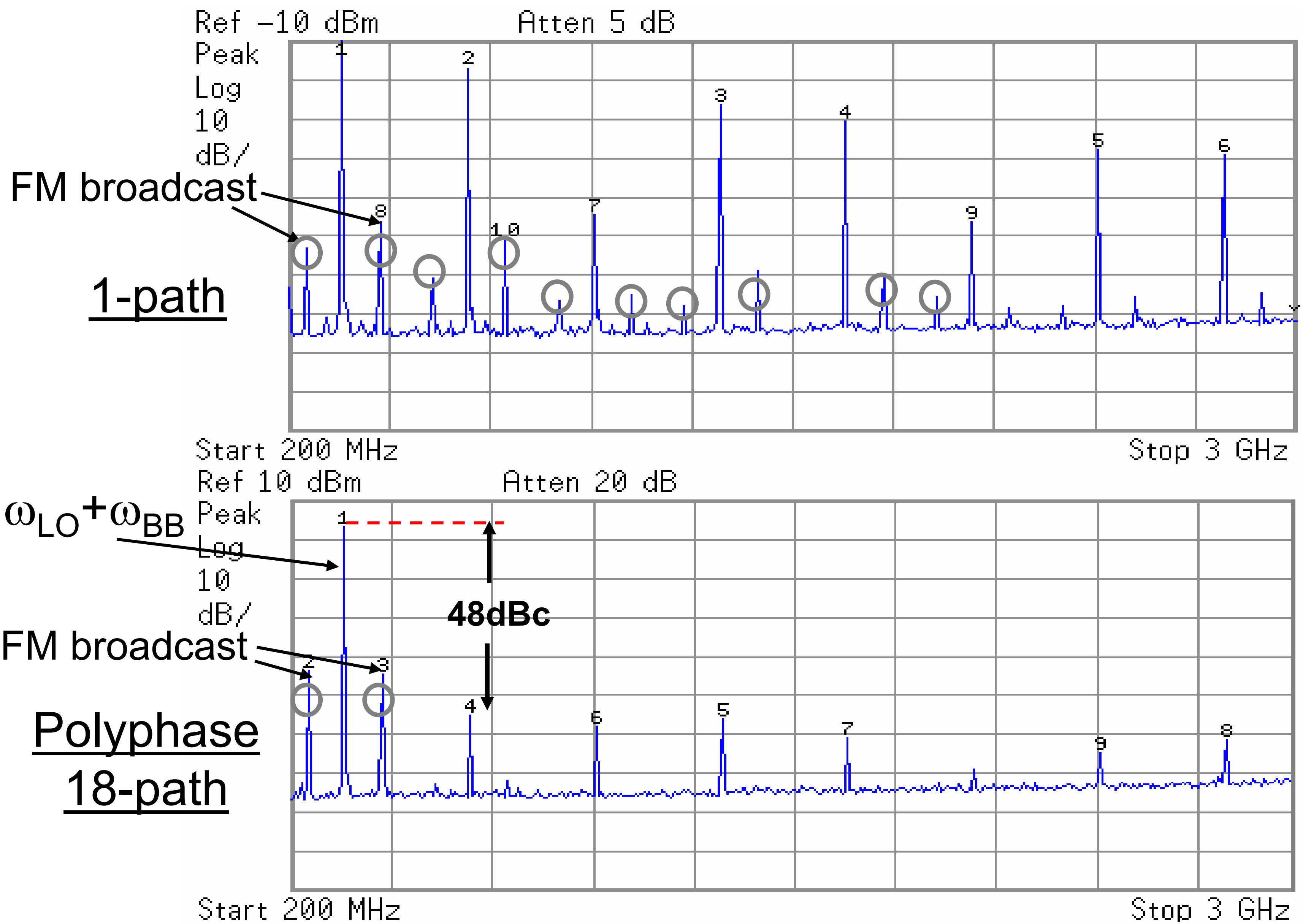


Flexible setup,18-path and 6-path mode

Technology: 1.2V, 0.13μm, 6M Copper CMOS

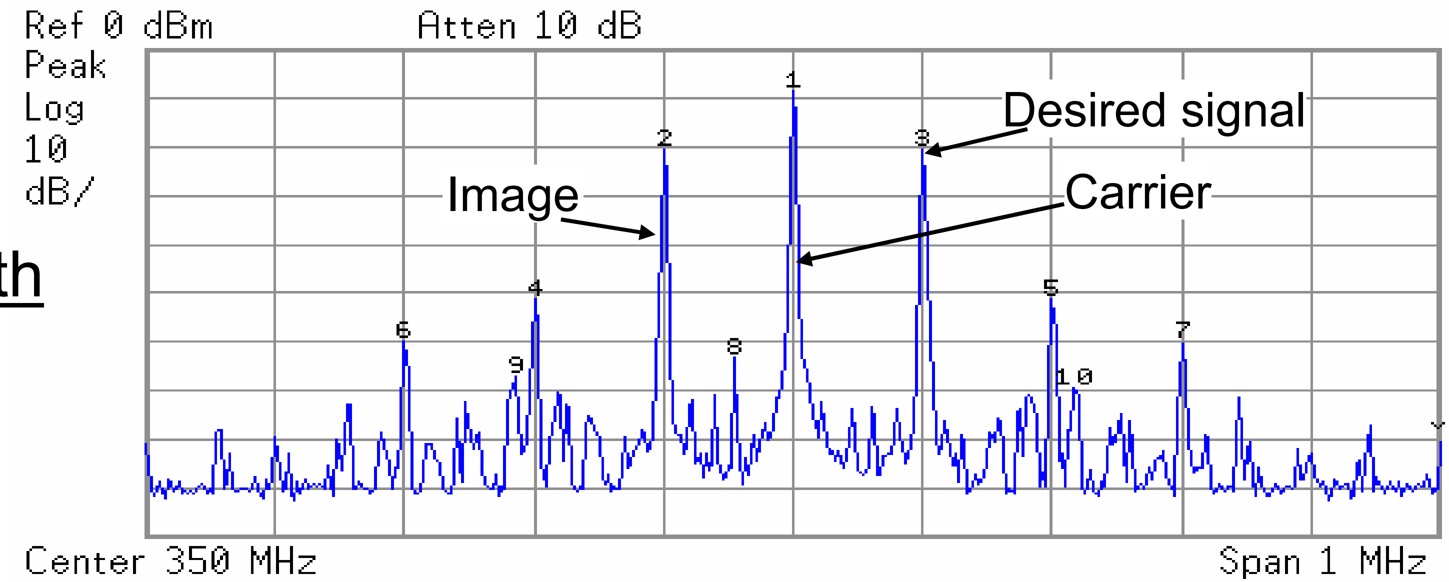
Active Area: $0.14mm^2$

Measurement Results

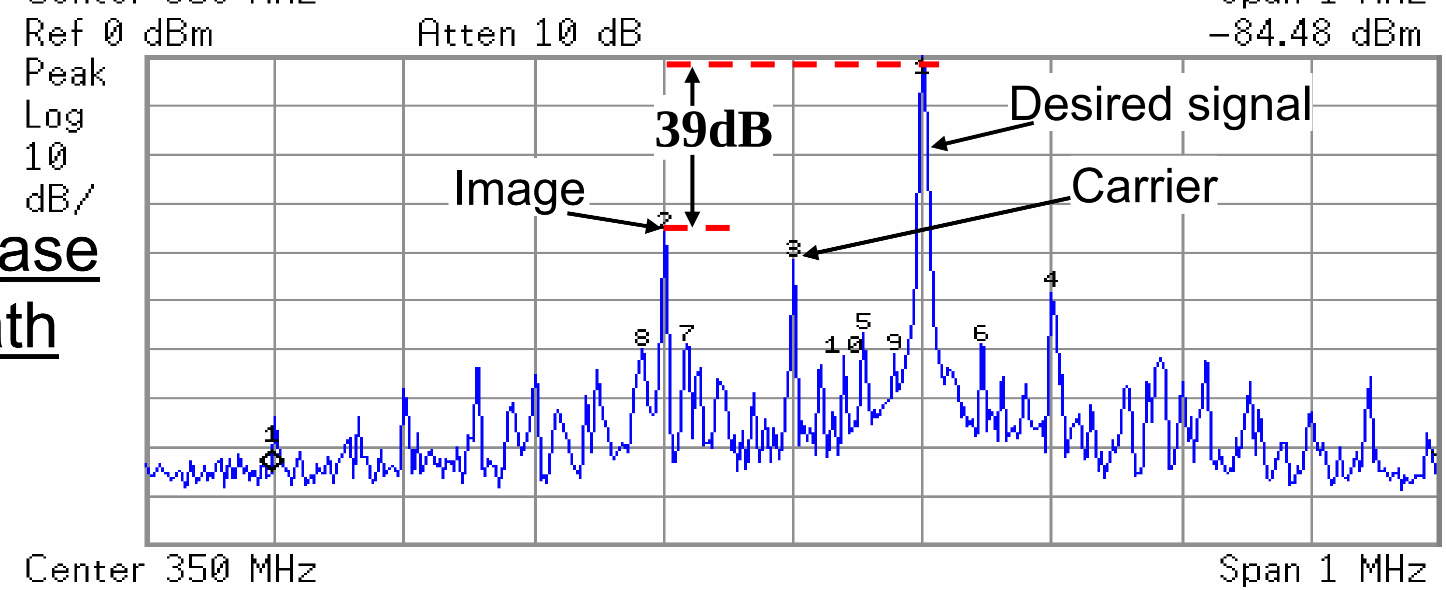


LO leakage and Image Rejection

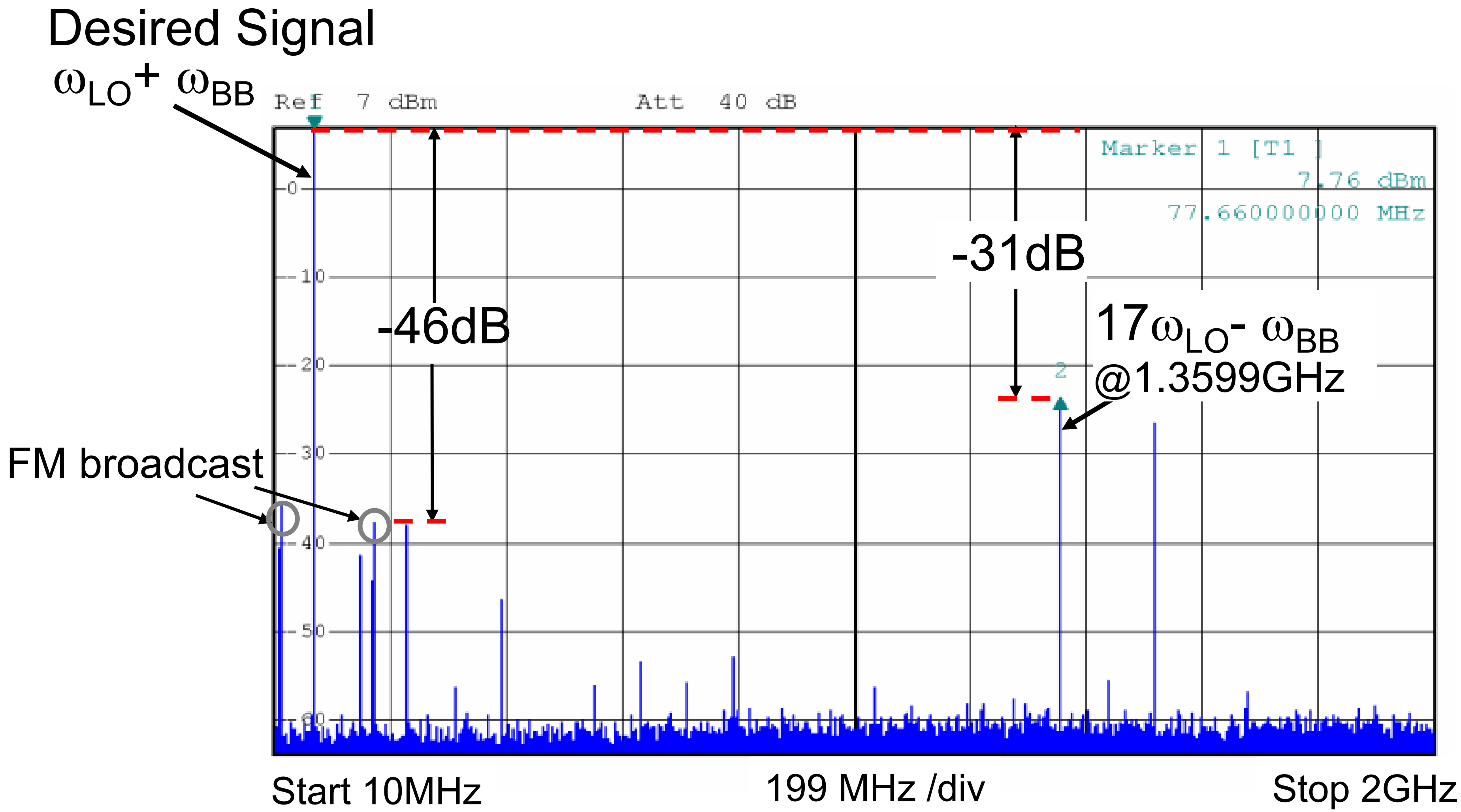
1-path



Polyphase
18-path



Full Spectrum (80MHz Carrier)



Other Performance

Technology		0.13μm CMOS
Supply Voltage		1.2V
Output Power		8mW
Output Swing		$2.54V_{pp\text{-}diff}$
Load		100Ω (diff)
Power Consumption	Digital circuits	156mW
	PU core	72mW
	Total	228mW
Worst case Harmonic Rejection (20 samples)		-40dBc

Summary: distortion canceling

- Polyphase multipath technique cancels harmonics and sidebands to relax or eliminate filters

- Wideband *filter-less* power upconverter with a clean output spectrum with digital circuits and mixers only

- Demonstrator IC operates from DC to 2.4GHz with worst case harmonic < -40dBc (20 samples)

- Useful for Software Defined Radio applications

reference

- R. Shrestha, E.A.M Klumperink, E. Mensink, G.J.M. Wienk, B. Nauta, "A Polyphase Multipath Technique for software Defined Radio Transmitters"IEEE Journal of Solid State Circuits, Vol. 41, No. 12, pp. 2681-2692, Dec. 2006.

Outline

- Introduction
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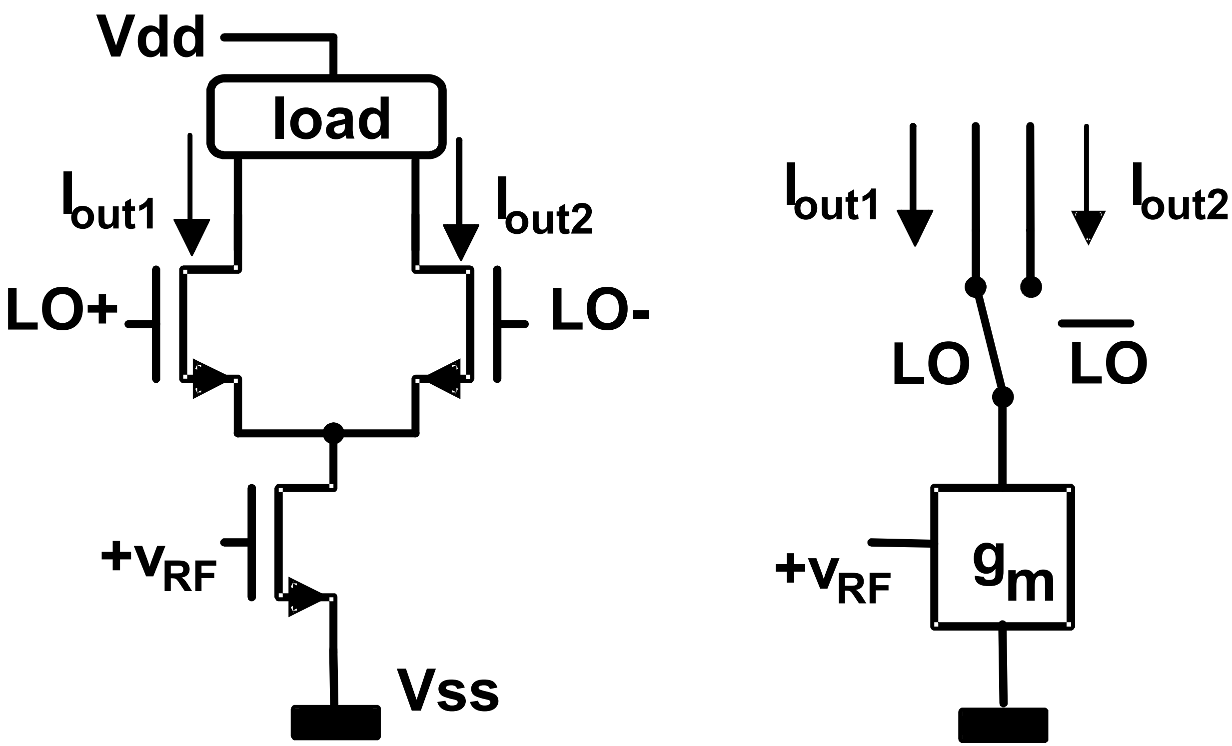
  - Distortion canceling
  - **Switched Gm mixer**

Switched transconductor mixer

- Alternative for Gilbert / passive mixer
- Operates at lower supply voltage

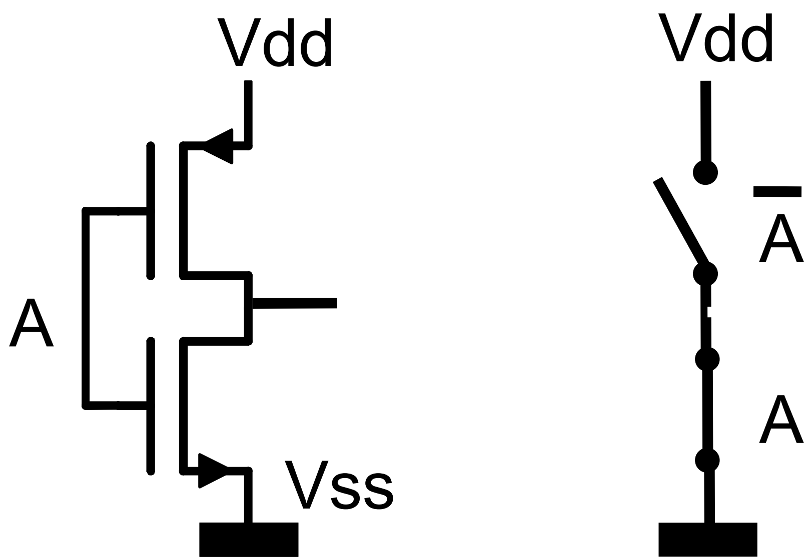
Essential Active Mixer Functions



Keep: Transconductance g_m and Switching!

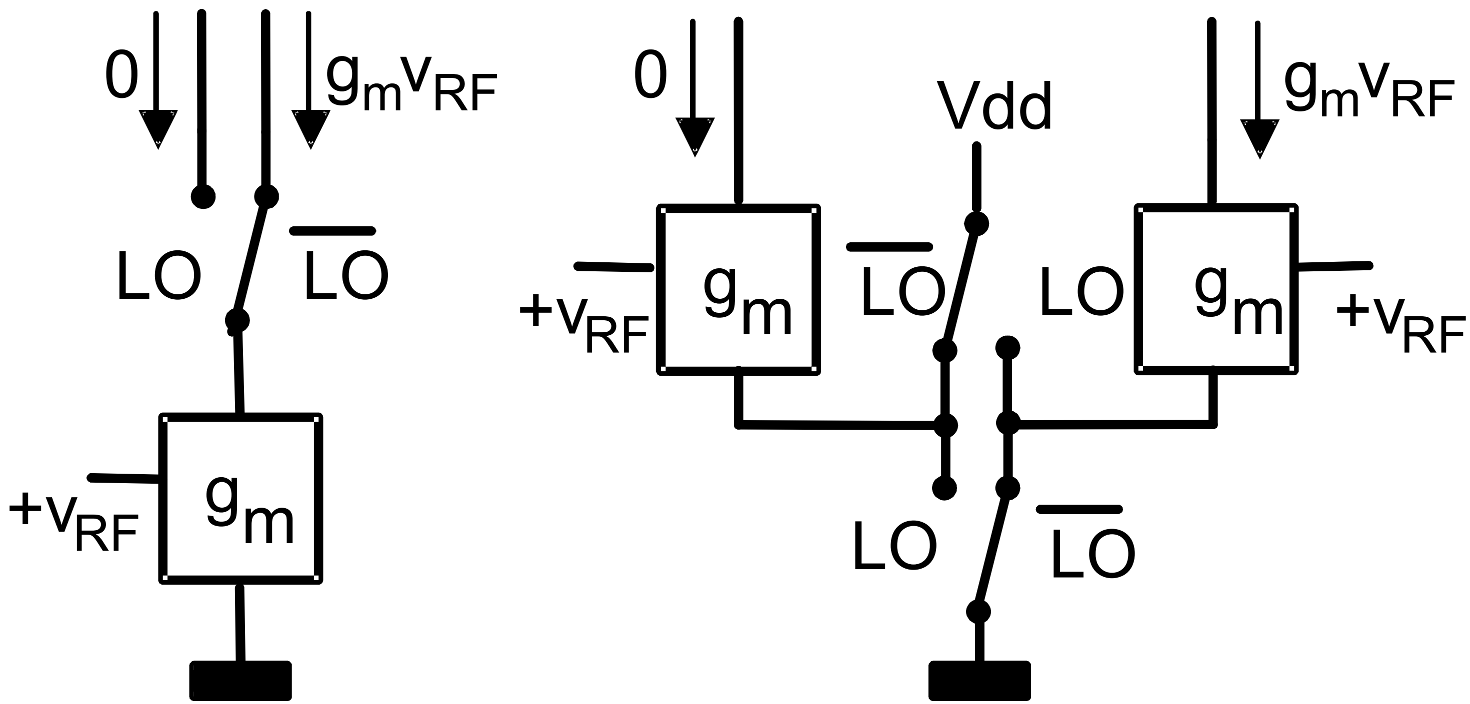
Use Only Switches to Supply!!

This will also work in future CMOS:



Good switch to Vss (N) and to Vdd (P)!

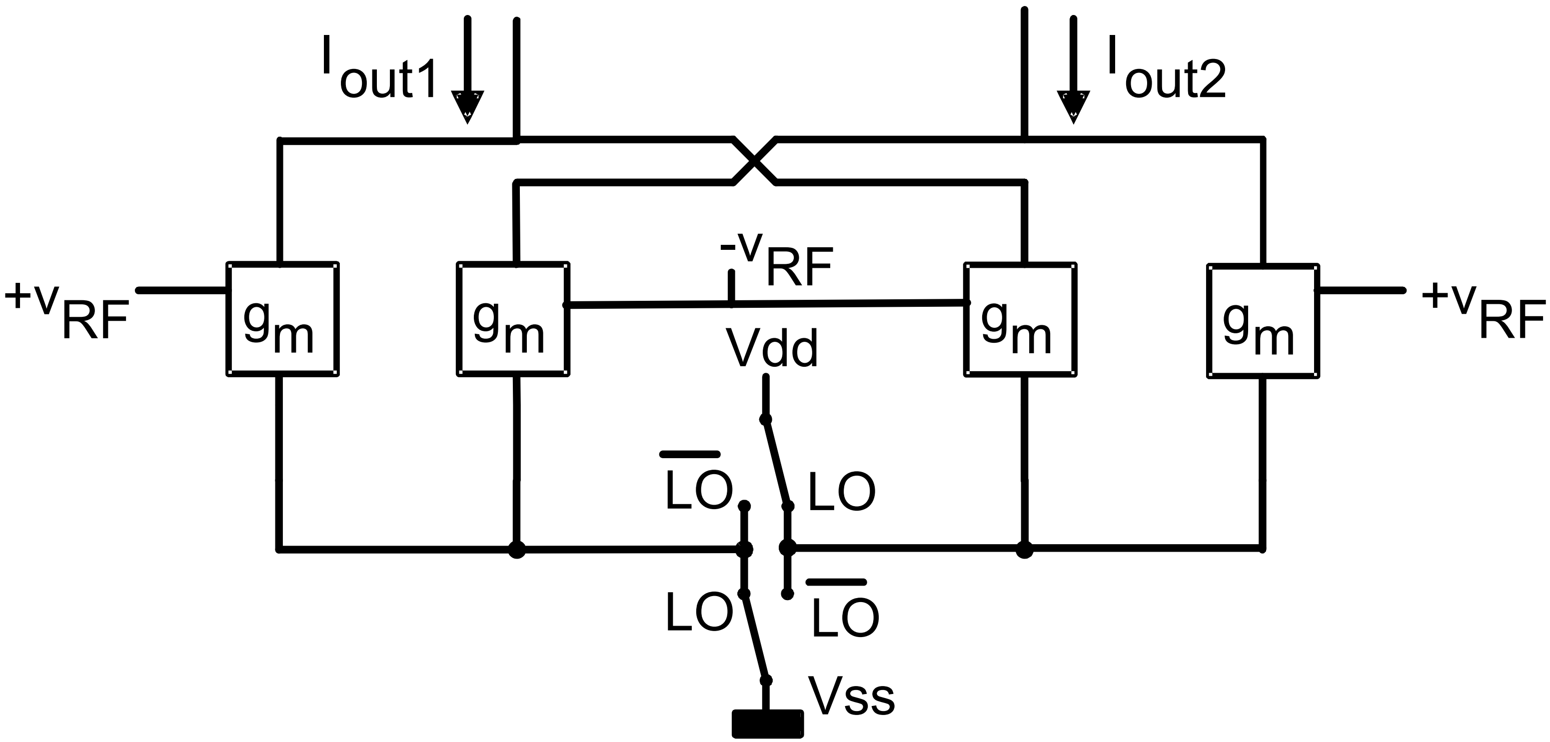
Complete Mixer



Traditional: switch current after V - I conversion

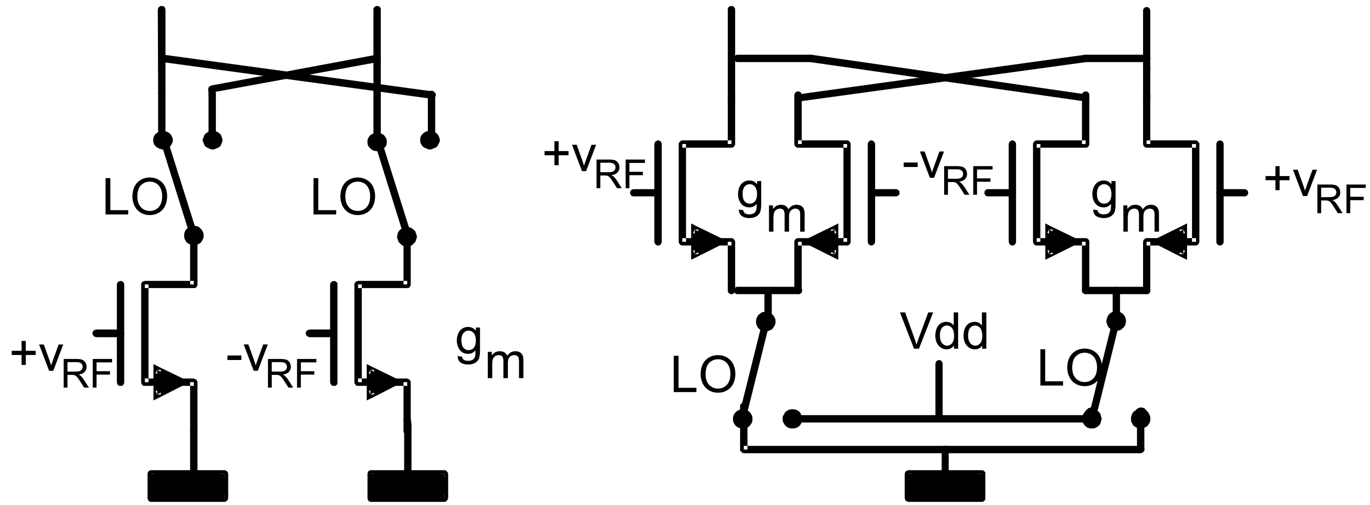
New mixer: Switch the Transconductors on/off!

Double Balanced Version



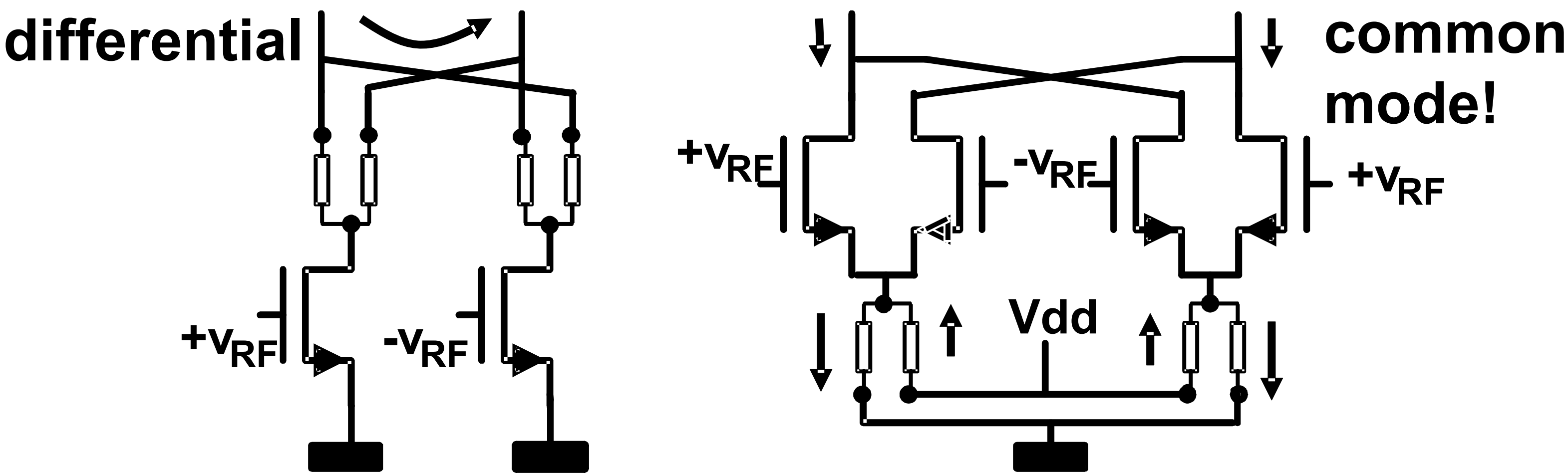
Add 2 identical transconductors with anti-phase RF-inputs and cross-coupled IF-outputs

Traditional Versus Switched g_m



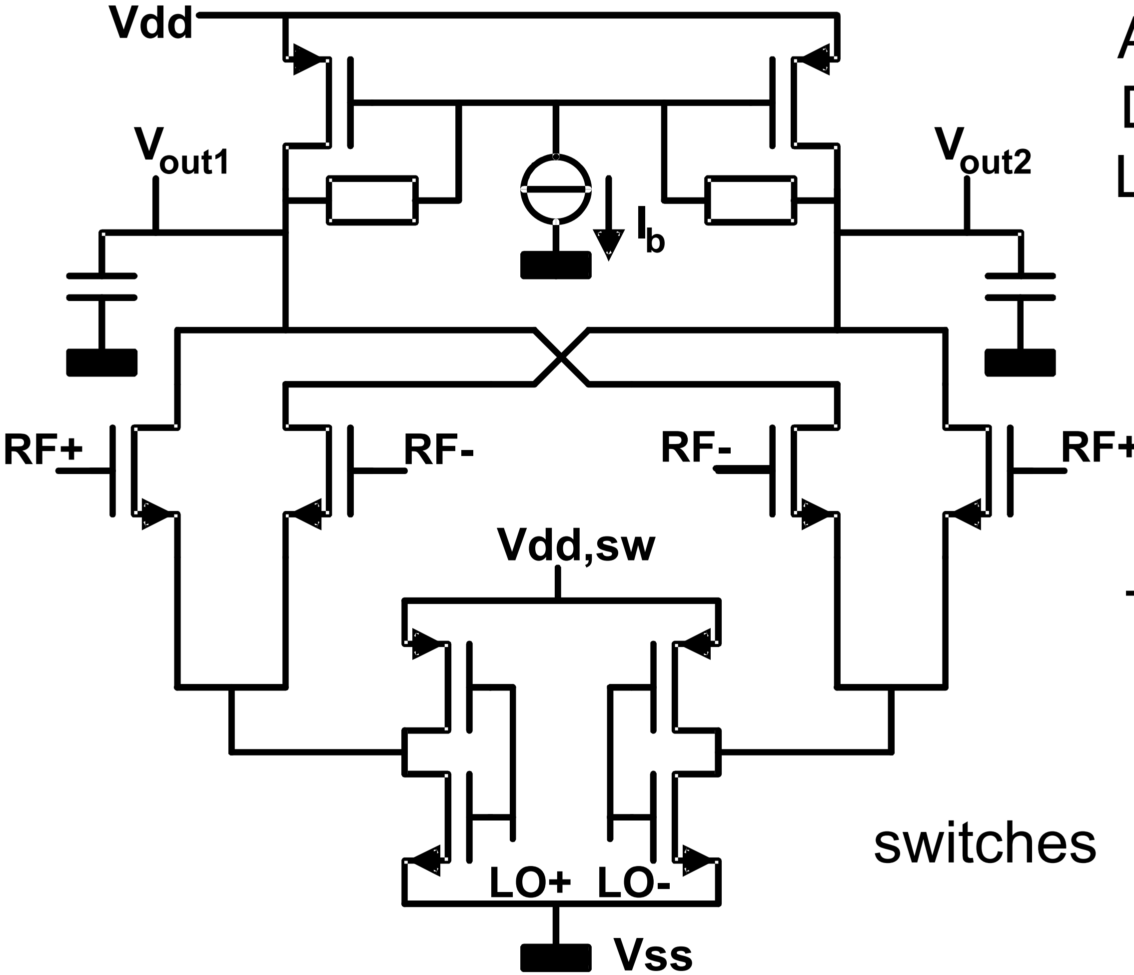
Property	Traditional	Switched g_m
conversion gain	$g_m \cdot 2/\pi$	$g_m \cdot 2/\pi$
Minimum V_{LO}	Vds,gm + Vgs,switch	Vgs,switch
thermal noise of g_m 1/f noise of g_m	$\sim g_m$ mixed up	$\sim g_m$ partly mixed up
Noise of switch /LO	....	....

Switches/LO Noise at 0- crossing



Property	Traditional	Switched gm
conversion gain	gm · 2/π	gm·2/π
Minimum VLO	Vds,gm + Vgs,switch	Vgs,switch
thermal noise gm	~ gm	~ gm
1/f noise of gm	mixed up	partly mixed up
Noise of switches/LO	differential IF noise	rejected (common)

Circuit Realized On Chip

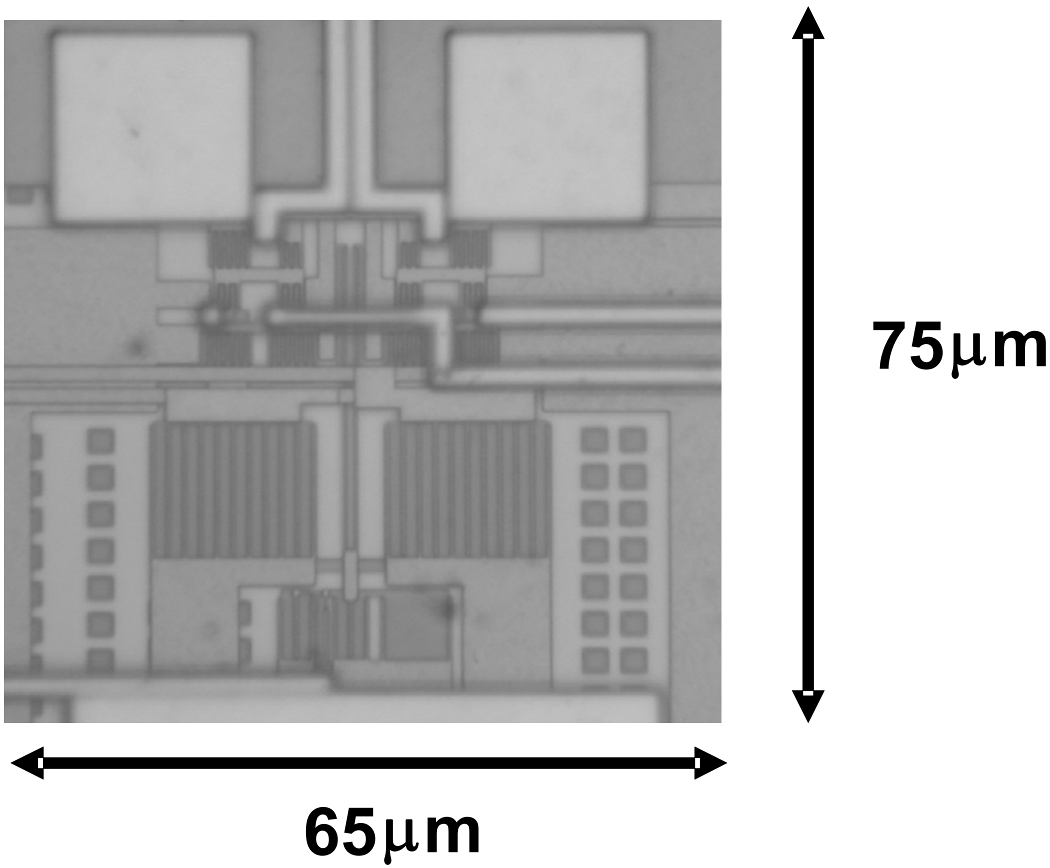


Absorb I-common,
Differential I-V,
Low-pass filter

Switched
Transconductors

switches

Mixer Core (0.18 μCMOS)



Summary: Switched transconductor mixer

New mixer concept:

- 12dB gain, 4GHz active mixer at Vdd=1Volt demonstrated in 0.18μm CMOS
- 15dB NF_{50} @1 GHz, 4mW

reference

- Klumperink, E.A.M., Louwsma, S.M., Wienk, G.J.M., Nauta, B. "A CMOS Switched Transconductor Mixer" IEEE Journal of Solid-State Circuits, Vol. 39, No. 8, pp. 1231-1240, August 2004.

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We're done!

Summary

- RF System trend
  - Wideband ICs
  - Multistandard & Software defined radio
- CMOS Technology trend
  - Nonlinearly operating transistors
  - Leaking gates
  - Low V_{dd}

Summary: Circuit Innovations

- Noise canceling
  - Creates degree of freedom
  - Low noise in wideband circuits possible without feedback
- 1/f noise reduction
  - Reduce 1/f noise at device level
- Distortion canceling
  - Multipath can cancel many harmonics
- Switched Gm mixer
  - Low V_{dd} operation possible